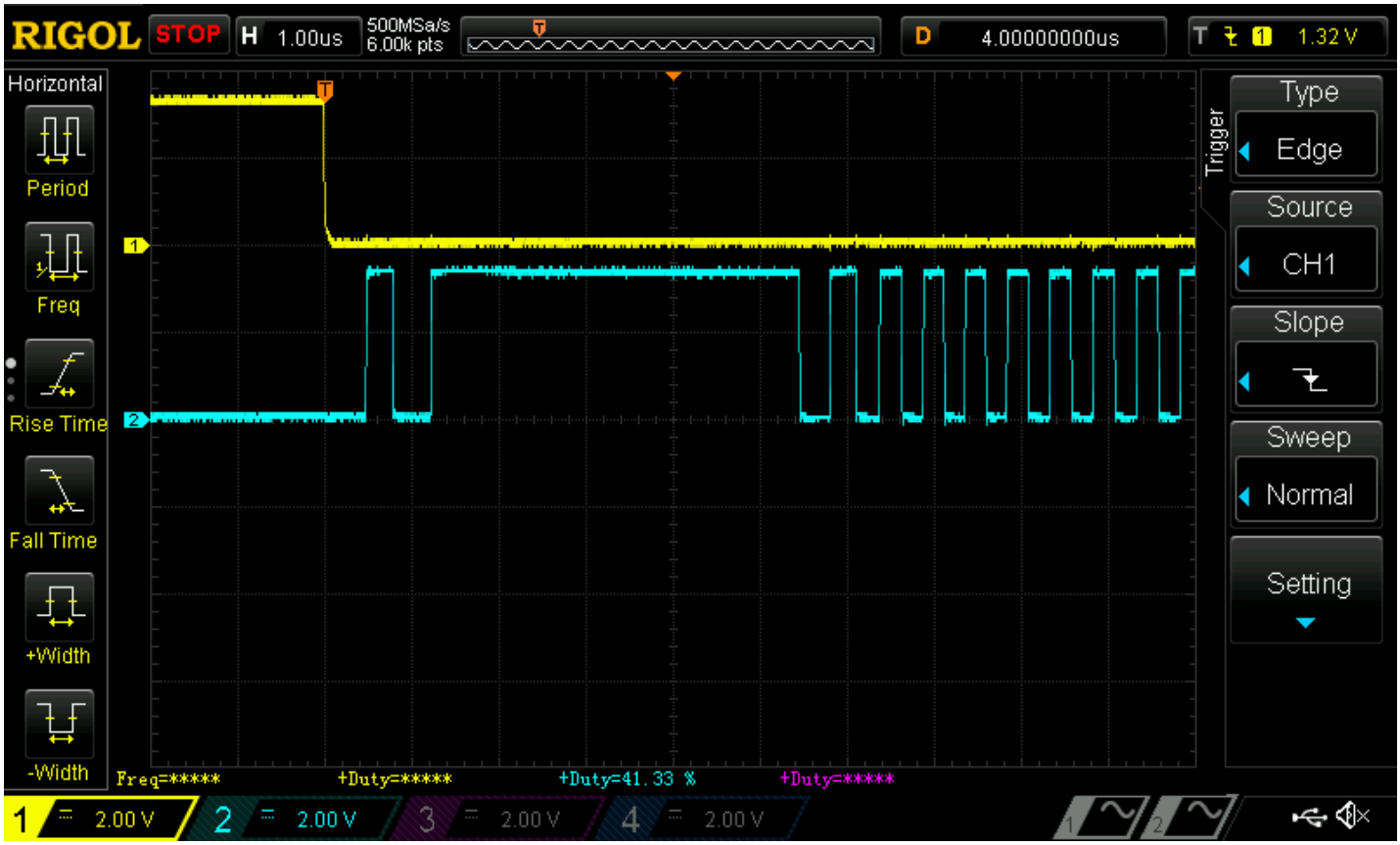
Errata disclaimer: This Errata applies to SLG46580V revision XC.

ISSUE 1: Long 2 MHz OSC Settling Time
Functional Block Affected: OSC, Counter, Delay
Description:

2MHz OSC has an additional ~ 9 cycles settling period. Higher VDD shows longer settling time.



Channel 1 – OSC Power Down; Channel 2 –OSC output

Such behavior will lead to substantial error in period calculations if the delay time is relatively small.

Workaround:

- Enable Fast Start-up option. Fast Start-up means forcing bias ready at the power-up instead of automatic enabling at OSC event. The standby current consumption difference between Fast start-up disabled and enabled is only an additional 300 nA.
- Use the “Force power on” OSC power control option to make the OSC operate at all times. However, this will cause increased constant current consumption.

ISSUE 2: Possible Glitch on ACMP Output
Functional Block Affected: ACMP

Description:

After power-up, if LDO is enabled earlier than ACMP, its output may generate a glitch.

VDD = 5.0 V, ACMP IN+ > IN-, One of LDOs enabled

Because BG_OK is already released by LDO, there is no gating signal. Depending on the ACMP VREF condition & the positive input value, it is possible for the ACMP to have a glitch. Subsequently, the other ACMP will not have an issue unless the customer repeats LDO enable first and ACMP later during power stable.

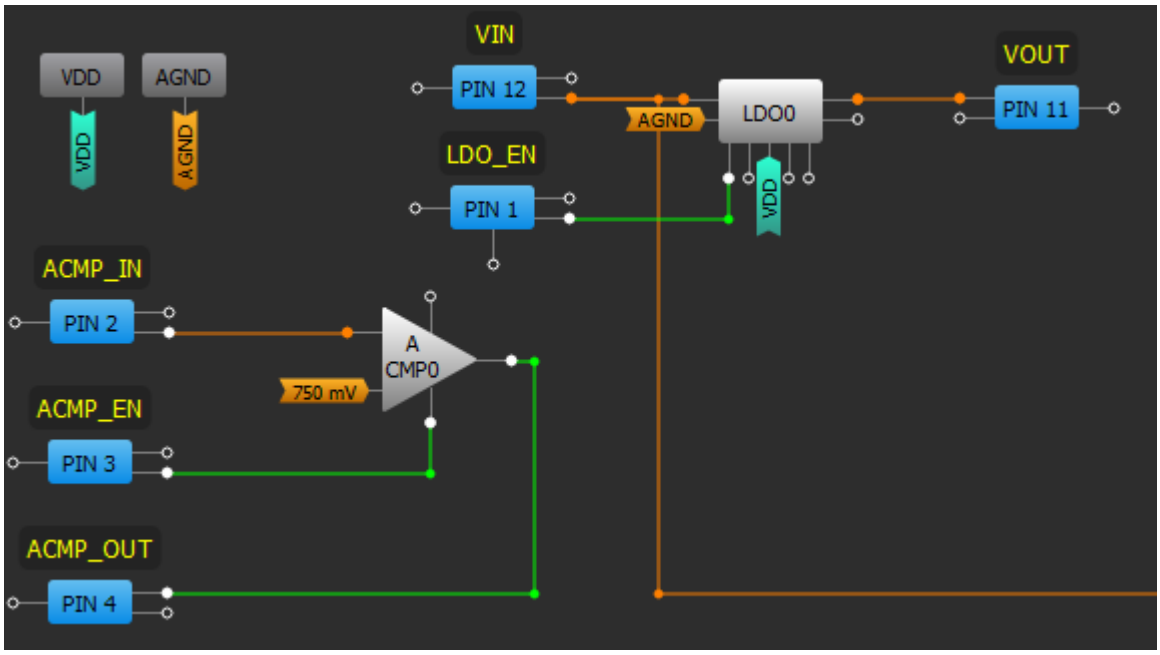
Workaround:

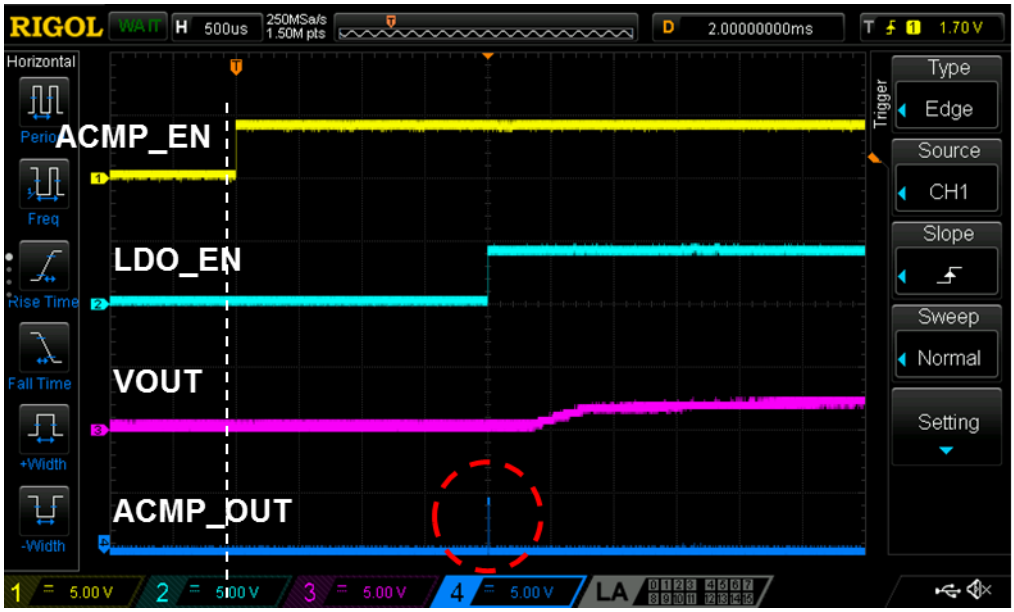
- Use both edge delay on the output to filter out the glitch.

ISSUE 3: Possible Glitch on ACMP Output
Functional Block Affected: ACMP

Description:

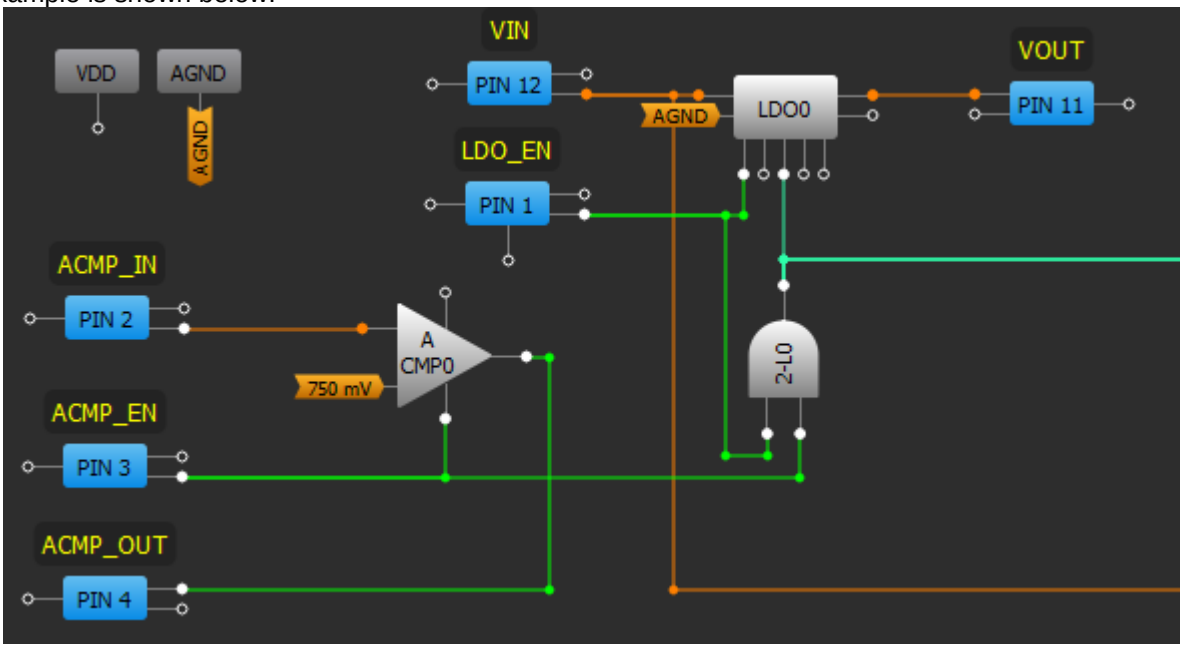
If an LDO's Low Power Mode is selected (for example tied to VDD) a glitch may appear on the ACMP's output after the first LDO is enabled. When the first LDO is turned on, the Low Power Mode switch causes a drop in the internal bandgap voltage that is used to derive the ACMP reference voltages.


VIN
VDD
AGND
PIN 12
VOUT
PIN 11
AGND
LDO0
LDO_EN
PIN 1
VDD
ACMP_IN
PIN 2
A
CMP0
750 mV
ACMP_EN
PIN 3
ACMP_OUT
PIN 4


RIGOL
WAIT
H 500us
250MSa/s
1.50M pts
D 2.00000000ms
T 1.70 V
Horizontal
Period
Freq
Rise Time
Fall Time
+Width
-Width
ACMP_EN
LDO_EN
VOUT
ACMP_OUT
Trigger
Type
Edge
Source
CH1
Slope
Sweep
Normal
Setting
1 5.00 V
2 5.00 V
3 5.00 V
4 5.00 V
LA

Workaround:

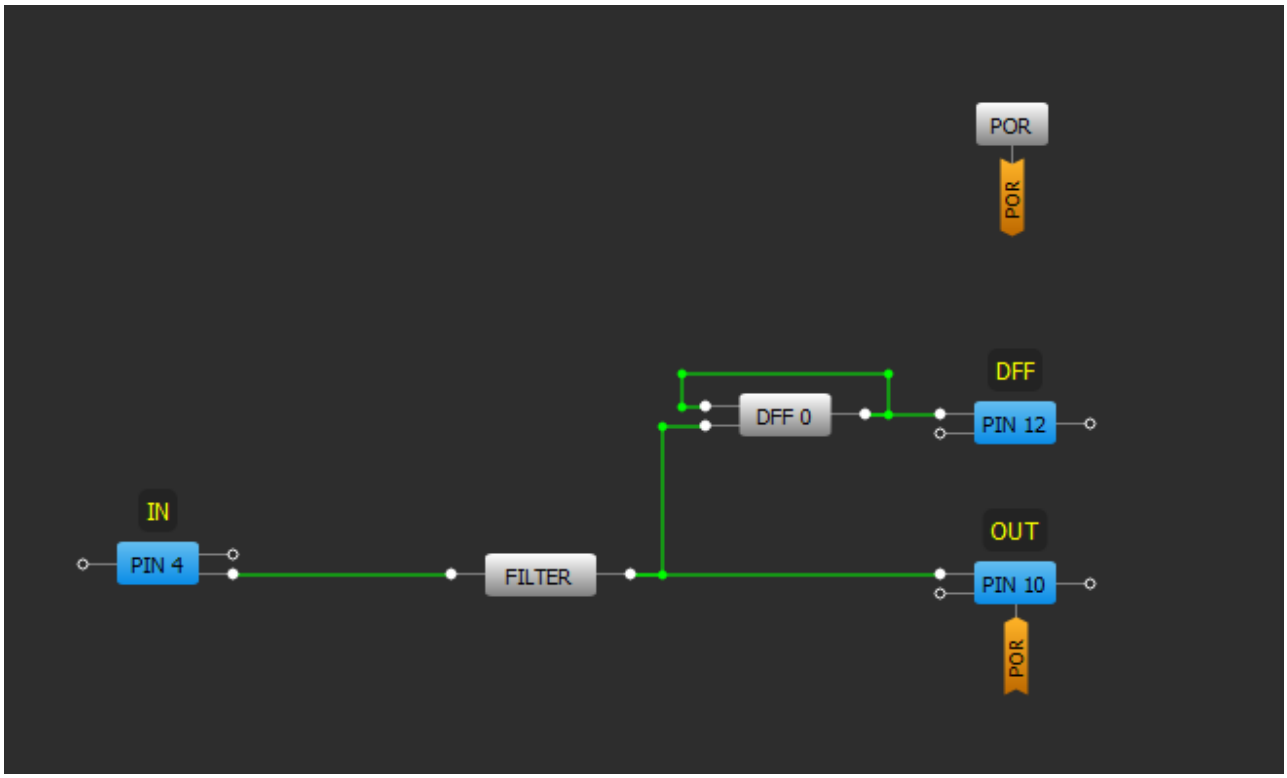
- Use both edge delay on the output to filter out the glitch.
- Use some logic to avoid turning on Low Power Mode before enabling LDO and powering up the ACMP. Example is shown below.



ISSUE 4: FILTER cell does not filter out glitches
Functional Block Affected: FILTER

Description:

If clock type high frequency input comes in, the FILTER cell may not filter out it. There are several factors like input frequency, duty cycle and LOW duration in such signal that may lead to its passing through FILTER block.



Channel 1 (yellow/top line) – PIN#4 (IN)
Channel 2 (light blue/2nd line) – PIN#10 (OUT)
Channel 3 (magenta /3rd line) – PIN#12 (DFF)

1. Period is 60ns. Pulse width is 10ns DC=16.7% (Correct functionality)

2. Period is 60ns. Pulse width is 20ns DC = 33.3% (Incorrect functionality)

3. Period is 60ns. Pulse width is 30ns DC=50% (Incorrect functionality)

4. Period is 60ns. Pulse width is 40ns DC=66.67% (Correct functionality)

Workaround:
Currently there is no workaround for this issue. Filter block is good at filtering short spontaneous glitches. It is intended to be used in series connection before the delay cell to avoid its latching (see issue #4).

Silego Technology
Corporate Headquarters
1515 Wyatt Drive
Santa Clara, CA 95054
USA
Phone: 408-327-8800

Silego Taiwan Office (Hsin Chu)
6F-12, Number 38, Tai Yuan Street
Tai Yuan Industrial Park, Jhubei City
Hsin Chu County, 30265, Taiwan
Phone: +886-3-560-0313
Fax: +886-3-560-0316

Silego Taiwan Office (Taipei)
9F, No.10, Ln. 321,Yangguang St,
Neihu District,
Taipei City 114, Taiwan
Phone: +886-2-2658-1038

Silego Japan Office
20F Shinjuku i-Land Tower
6-5-1 Nishi-shinjuku, Shinjuku-ku,
Tokyo 163-1320
Phone: 03-6830-5035
Fax: 03-3348-7515

Silego Korea Office (Seoul)
#402 Dongmun Building, 10,
Dogok-ro 2-gil, Gangnam-gu,
Seoul, Korea (Post code: 06258)
Phone: +82-3453-7560 or
+82-2-3453-7127

Silego Korea Office (Suwon)
#101-801 Hanwha-Ggumegreen-Hyowon,
1116-3 Ingye-dong, Paldal-gu,
Suwon-si, Gyeonggi-do, Korea

Silego China Office (Hefei)
Rm303, Building 2, No3 TianYuan Rd
High-Tech Zone
Hefei, China 230088
Phone: +86-551-65368431
Fax: +86-551-65368432

Silego Ukraine Office
Business Center Intercity-Silego
Chervonoi Kalyny ave., 62a, 5th Floor, Room 5.1
Lviv, Ukraine
Phone: +38(032)232-80-53