SLG59M1640V

Ultra-small 2-Channel 45 mΩ/2 A Power Switch with Reverse-Current Blocking

General Description

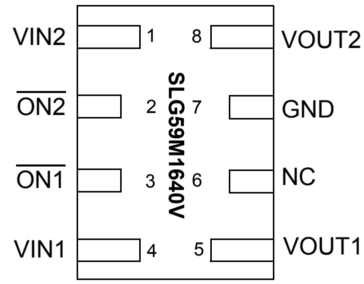
The SLG59M1640V is a dual-channel, 45 mΩ PMOS power switch designed to switch 1.5 to 5 V power rails up to 2 A in each channel. When either channel is enabled, reverse-current protection will quickly open the switch in the event of a reverse-voltage condition is detected (a $V_{OUT} > V_{IN} + 50$ mV condition opens the switch). In the event that the channel's V_{IN} voltage is too low, the power switch also contains an internal UVLO threshold monitor to keep or to turn the switch OFF. For fast load turnoff when either switch is disabled ($\overline{ONx}$ = LOW-to-HIGH), each channel has its own fast discharge transistor that connects an internal 150 Ω RDS_{ON} transistor to ground. Each power switch is independently controlled via its own low-voltage compatible CMOS input.

Designed to operate over a -40°C to 85°C range, the SLG59M1640V is available in a RoHS-compliant, ultra-small 1.6 x 1.0 mm STDFN package.

Features

- Integrated 2-Channel PMOS Power Switch
- 2 A Maximum Continuous Switch Current per Channel
- Low RDS_{ON}:
  - 45 mΩ at V_{IN} = 5 V
  - 60 mΩ at V_{IN} = 2.5 V
  - 75 mΩ at V_{IN} = 1.5 V
- Operating Voltage: 1.5 V to 5.5 V
- Reverse-current/voltage Protection
- Fast Output Discharge
- Low-voltage CMOS Logic Compatible Switch Control
- Operating temperature range: -40 °C to 85°C
- Pb-Free / Halogen-Free / RoHS compliant packaging

Pin Configuration

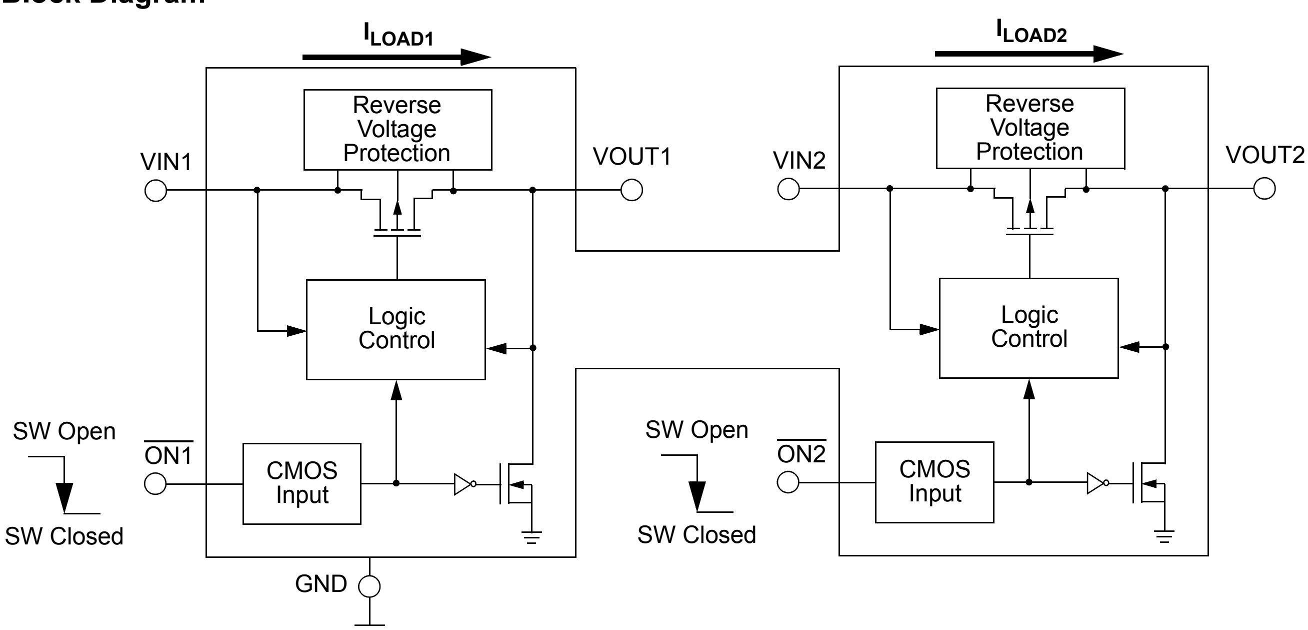


8-pin STDFN
(Top View)

Applications

- Power-Rail Switching:
  - Notebook/Laptop/Tablet PCs
  - Smartphones/Wireless Handsets
  - High-definition Digital Cameras
  - Set-top Boxes
- Point of Sales Pins
- GPS Navigation Devices

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
1	VIN2	MOSFET	Input and source terminal of MOSFET #2. Bypass the VIN2 pin to GND with a 10 µF (or larger), low-ESR capacitor.
2	$\overline{ON2}$	Input	$\overline{ON2}$ turns Channel 2 MOSFET ON and is a low logic-level CMOS input with V_{IL} < 0.3 V and V_{IH} > 1 V. As the ON2 input circuit does not have an internal pull-down resistor, connect ON2 pin directly to a GPIO controller – do not allow this pin to be open circuited.
3	$\overline{ON1}$	Input	$\overline{ON1}$ turns Channel 1 MOSFET ON and is a low-logic level CMOS input with V_{IL} < 0.3 V and V_{IH} > 1 V. As the ON1 input circuit does not have an internal pull-down resistor, connect ON1 pin directly to a GPIO controller – do not allow this pin to be open circuited.
4	VIN1	MOSFET	Input and source terminal of MOSFET #1. Bypass the VIN1 pin to GND with a 10 µF (or larger), low-ESR capacitor.
5	VOUT1	MOSFET	Output and drain terminal of MOSFET #1.
6	NC	No Connect	No connection. Do not make connection to any other pin - leave Pin 6 as an open circuit.
7	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.
8	VOUT2	MOSFET	Output and drain terminal of MOSFET #2.

Ordering Information

Part Number	Type	Production Flow
SLG59M1640V	STDFN	Industrial, -40 °C to 85 °C
SLG59M1640VTR	STDFN (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Power Supply		-0.3	--	6	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	1000	--	--	V
MSL	Moisture Sensitivity Level			1		
θ_{JA}	Thermal Resistance	1.0 x 1.6 mm 8L STDFN	--	82	--	°C/W
$T_{J,MAX}$	Maximum Junction Temperature		--	150	--	°C
MOSFET IDS_{CONT}	Continuous Current from VIN to VOUT	Each channel, TJ< 150°C	--	--	2	A
MOSFET IDS_{PK}	Peak Current from Drain to Source	Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle	--	--	2.5	A
Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.						

Electrical Characteristics

1.5V ≤ $V_{IN[1,2]}$ ≤ 5.5V; C_{IN} = 10µF, T_A =-40 °C to 85 °C, unless otherwise noted.
Typical values are at T_A = 25°C (unless otherwise stated)

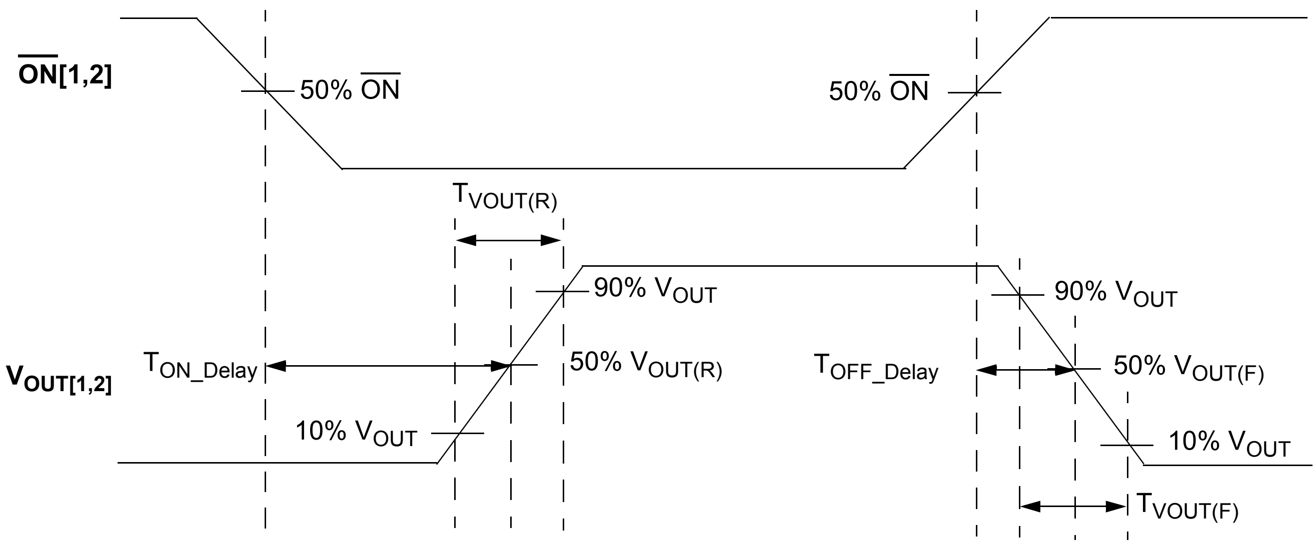
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{IN[1,2]}$	Switch Input Voltage		1.5	--	5.5	V
$V_{IN(UVLO)}$	VIN Undervoltage Lockout Threshold	V_{IN} ↑, $V_{\overline{ON}}$ = 0V, I_{OUT} = -100 mA	--	--	1.2	V
		V_{IN} ↓, $V_{\overline{ON}}$ = 0V, R_{LOAD} = 10 Ω	0.5	--	--	V
I_{IN}	Quiescent Supply Current, Both Channels	V_{IN} = 5.25V, $V_{\overline{ON}}$ = LOW, I_{OUT} = 0 mA	--	3.5	5.3	µA
		V_{IN} = 1.5V, $V_{\overline{ON}}$ = LOW, I_{OUT} = 0 mA	--	2.5	4	µA
$I_{IN(OFF)}$	OFF Mode Supply Current, Both Channels	V_{IN} = 5.25V, $V_{\overline{ON}}$ = V_{IN}, R_{LOAD} = 1 MΩ	--	1	1.5	µA
		V_{IN} = 1.5V, $V_{\overline{ON}}$ = V_{IN}, R_{LOAD} = 1 MΩ	--	0.4	1	µA
RDS_{ON}	Static Drain to Source ON Resistance	T_A = 25°C, V_{IN} = 5.0 V, I_{LOAD} = -200 mA	--	45	55	mΩ
		T_A = 25°C, V_{IN} = 2.5 V, I_{LOAD} = -200 mA	--	60	72	mΩ
		T_A = 25°C, V_{IN} = 1.5 V, I_{LOAD} = -200 mA	--	80	96	mΩ
$V_{REVERSE}$	Reverse-current Voltage Threshold		--	50	--	mV
$I_{REVERSE}$	Reverse-current Leakage Current after Reverse Current Event	V_{IN} = 0 V, V_{OUT} = 1.5 V to 5.25 V; $V_{\overline{ON1}}$ = $V_{\overline{ON2}}$ = V_{OUT}; T_A = 25 °C	--	0.6	1.5	µA
$V_{\overline{ON}[1,2]}$	$\overline{ON}$ Pin Voltage Range		0	--	V_{IN}	V
$I_{ON(Leakage)}$	$\overline{ON}$ Pin Leakage Current	1.4 V ≤ $V_{\overline{ON}}$ ≤ 5.25 V or $V_{\overline{ON}}$ = GND	--	--	1	µA
ON_V_{IH}	$\overline{ON}$ Pin Input High Voltage		1	--	V_{DD}	V
ON_V_{IL}	$\overline{ON}$ Pin Input Low Voltage		-0.3	0	0.3	V

Electrical Characteristics (continued)

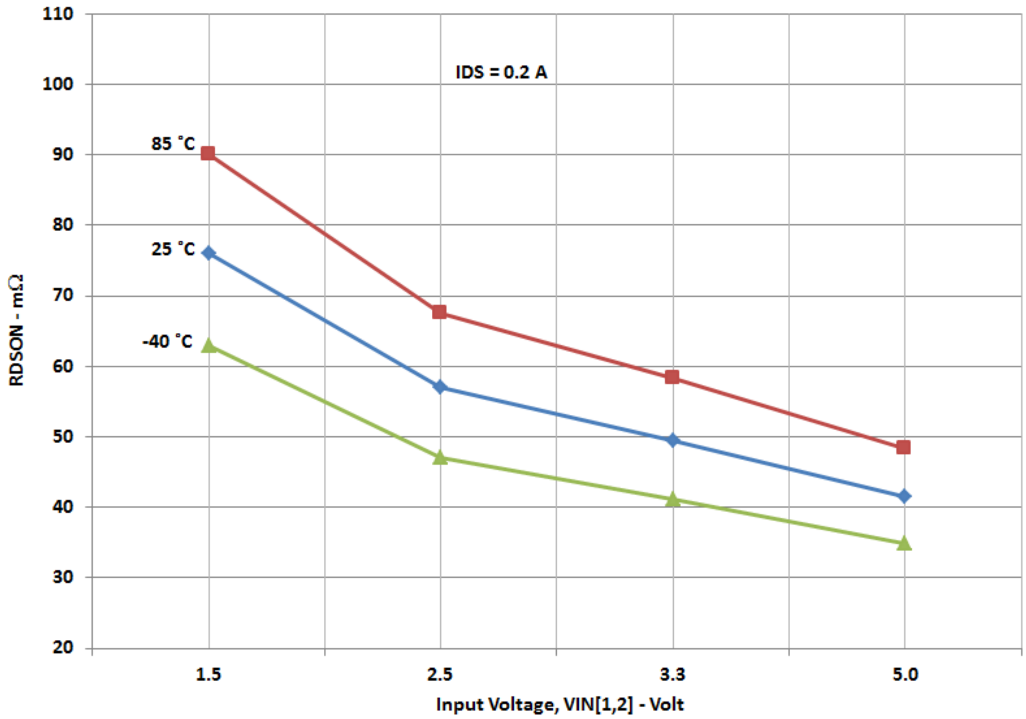
1.5V ≤ $V_{IN[1,2]}$ ≤ 5.5V; C_{IN} = 10µF, T_A =-40 °C to 85 °C, unless otherwise noted.
Typical values are at T_A = 25°C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
ON_{HYS}	$\overline{ON}$ Hysteresis		--	60	--	mV
RDSCHRG	Output Discharge Resistance	V_{IN} = 5 V, V_{OUT} = 0.4 V	0.1	0.18	0.25	kΩ
		V_{IN} = 1.5 V, V_{OUT} = 0.4 V	0.5	0.75	1	kΩ
T_{REV}	Reverse-current Detect Response Delay	V_{IN} = 5 V	--	10	--	µs
T_{REARM}	Reverse Detect Rearm Time		--	16	--	µs
T_{ON_Delay}	$\overline{ON}$[1,2] Delay Time	50% $\overline{ON}$ to 50% V_{OUTx} ↑; T_A = 25°C, V_{INx} = 5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	0.9	--	5	µs
		50% V_{IN} to 50% V_{OUTx} ↑; T_A = 25°C, V_{INx} = 1.5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	30	--	85	µs
$T_{VOUT(R)}$	VOUT[1,2] Rise Time	10% to 90% V_{OUTx} ↑; T_A = 25°C, V_{INx} = 5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	0.7	1.1	1.5	µs
		10% to 90% V_{OUTx} ↑; T_A = 25°C, V_{INx} = 1.5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	20	31	42	µs
$T_{VOUT(F)}$	VOUT[1,2] Fall Time	90% to 10% V_{OUTx} ↓; T_A = 25°C, V_{INx} = 5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	--	3	µs
		90% to 10% V_{OUTx} ↓; T_A = 25°C, V_{INx} = 1.5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	--	3.5	µs
T_{OFF_Delay}	OFF Delay Time	50% $\overline{ON}$ to 50% V_{OUT} ↓; T_A = 25°C, V_{IN} = 5V; R_{LOAD} = 10Ω, C_{LOAD} = 0.1µF	--	--	4.5	µs
		50% $\overline{ON}$ to 50% V_{OUT} ↓; T_A = 25°C, V_{IN} = 1.5 V; R_{LOAD} = 10 Ω, C_{LOAD} = 0.1 µF	--	--	5.2	µs

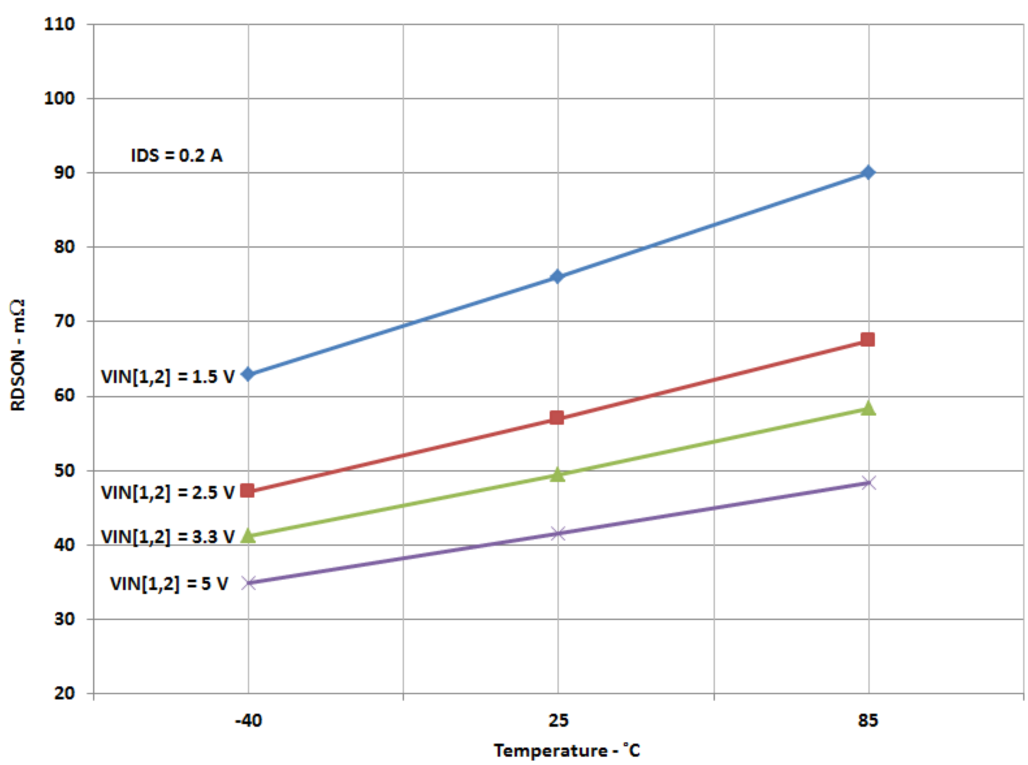
T_{Total_ON}, T_{ON_Delay} and Slew Rate Measurement



RDS_{ON} vs. $V_{IN[1,2]}$ and Temperature



RDS_{ON} vs.Temperature and $V_{IN[1,2]}$



$V_{IN[1,2]}$ Inrush Current Details

When either channel of the SLG59M1640V is enabled with ON[1,2] ↑, the power switch closes to charge the $V_{OUT[1,2]}$ output capacitor to $V_{IN[1,2]}$. The charging current drawn from VIN[1,2] is commonly referred to as “VIN inrush current” and can cause the input power source to collapse if the VIN inrush current is too high.

Since the $V_{OUT[1,2]}$ rise time of the SLG59M1640V is fixed, $V_{IN[1,2]}$ inrush current is then a function of the output capacitance at $V_{OUT[1,2]}$. The expression relating $V_{IN[1,2]}$ inrush current, the SLG59M1640V $V_{OUT[1,2]}$ rise time, and $C_{LOAD[1,2]}$ is:

$$V_{IN[1,2]} \text{ Inrush Current} = C_{LOAD[1,2]} \times \frac{\Delta V_{OUT[1,2]}}{V_{OUT[1,2]} \text{ Rise Time}}$$

where in this expression Δ $V_{OUT[1,2]}$ is equivalent to 0.8 x $V_{IN[1,2]}$ if the initial SLG59M1640V’s output voltages are zero.

In the table below are examples of $V_{IN[1,2]}$ inrush currents assuming zero initial charge on $C_{LOAD[1,2]}$ as a function of $V_{IN[1,2]}$.

$V_{IN[1,2]}$	$V_{OUT[1,2]}$ Rise Time	$C_{LOAD[1,2]}$	Inrush Current
1.5 V	31 µs	0.1 µF	3.8 mA
5 V	1.1 µs	0.1 µF	363 mA

Since the relationship is linear and If $C_{LOAD[1,2]}$ were increased to 1 µF, then the $V_{IN[1,2]}$ inrush currents would be 10x higher in either example. If a large $C_{LOAD[1,2]}$ capacitor is required in the application and depending upon the strength of the input power source, it may very well be necessary to increase the C_{IN}-to-C_{LOAD} ratio to minimize VIN[1,2] droop during turn-on.

For other $V_{OUT[1,2]}$ rise time options, please contact Silego for additional information.

Power Dissipation

The junction temperature of the SLG59M1640V depends on factors such as board layout, ambient temperature, external air flow over the package, load current, and the RDS_{ON}-generated voltage drop across each power MOSFET. While the primary contributor to the increase in the junction temperature of the SLG59M1640V is the power dissipation of its power MOSFETs, its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD_{TOTAL} = (RDS_{ON1} \times I_{DS1}^2) + (RDS_{ON2} \times I_{DS2}^2)$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

$RDS_{ON[1,2]}$ = Channel 1 and Channel 2 Power MOSFET ON resistance, in Ohms (Ω), respectively

$I_{DS[1,2]}$ = Channel 1 and Channel 2 Output current, in Amps (A), respectively

and

$$T_J = PD_{TOTAL} \times \theta_{JA} + T_A$$

where:

T_J = Die junction temperature, in Celsius degrees (°C)

θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W) – highly dependent on pcb layout

T_A = Ambient temperature, in Celsius degrees (°C)

Power Dissipation (continued)

In nominal operating mode, the SLG59M1640V's power dissipation can also be calculated by taking into account the voltage drop across each switch (V_{INx}-V_{OUTx}) and the magnitude of that channel's output current (I_{DSx}):

$$PD_{TOTAL} = [(V_{IN1}-V_{OUT1}) \times I_{DS1}] + [(V_{IN2}-V_{OUT2}) \times I_{DS2}] \text{ or}$$

$$PD_{TOTAL} = [(V_{IN1} - (R_{LOAD1} \times I_{DS1})) \times I_{OUT1}] + [(V_{IN2} - (R_{LOAD2} \times I_{DS2})) \times I_{DS2}]$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

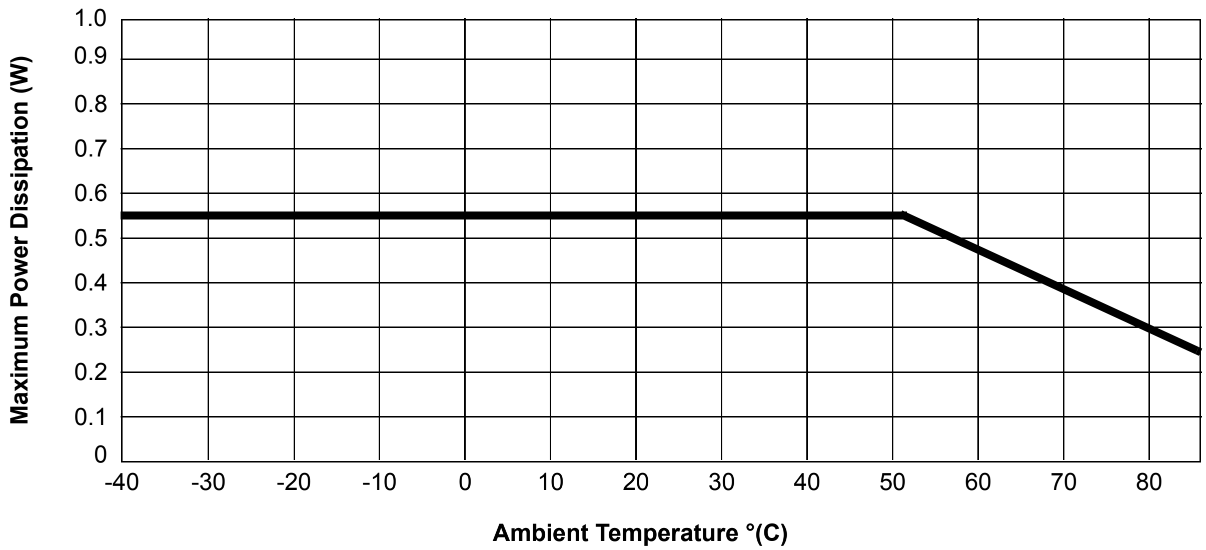
$V_{IN[1,2]}$ = Channel 1 and Channel 2 Input Voltage, in Volts (V), respectively

$R_{LOAD[1,2]}$ = Channel 1 and Channel 2 Output Load Resistance, in Ohms (Ω), respectively

$I_{DS[1,2]}$ = Channel 1 and Channel 2 output current, in Amps (A), respectively

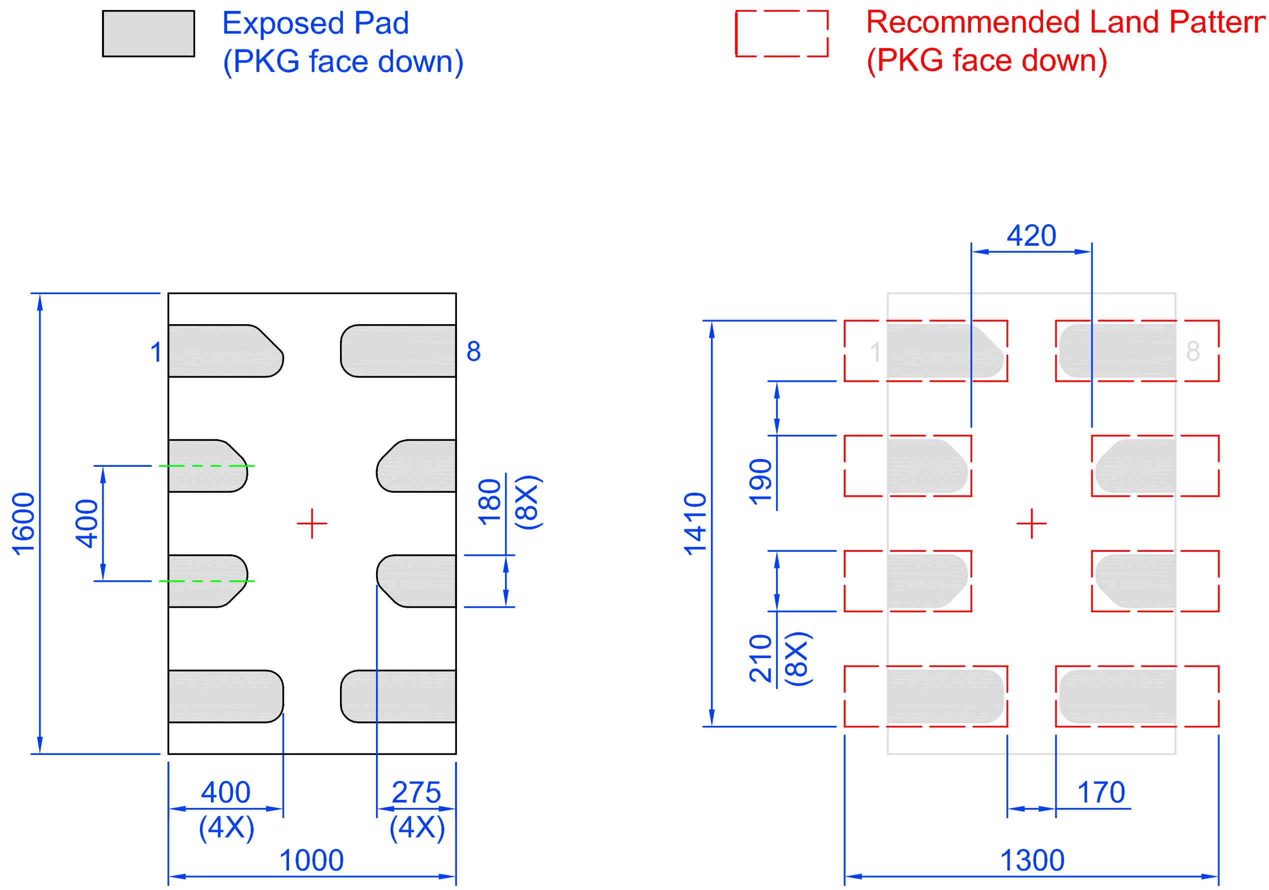
$V_{OUT[1,2]}$ = Channel 1 and Channel 2 output voltage, or $R_{LOAD[1,2]} \times I_{OUT[1,2]}$, respectively

Power Dissipation Derating Curve



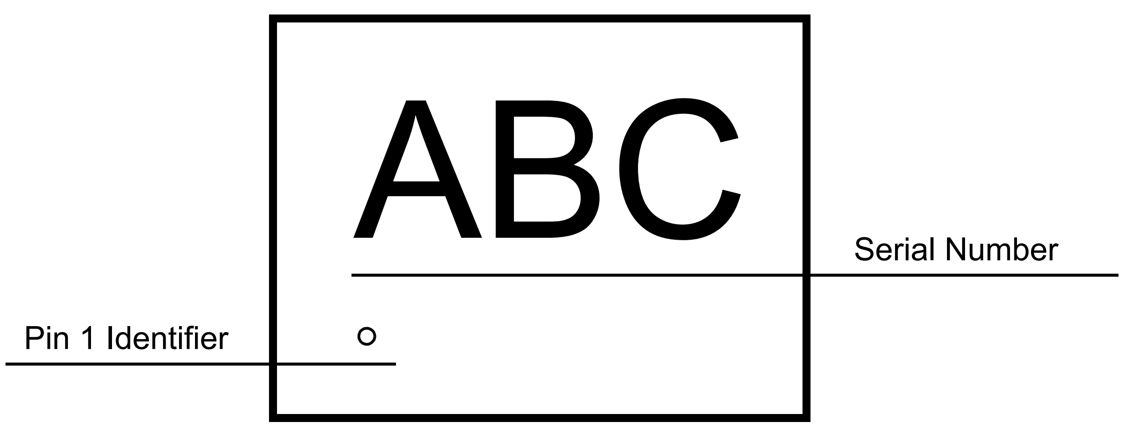
Note: Each V_{IN}, V_{OUT} = 1 in^2 1.2 oz. copper on FR4

SLG59M1640V Layout Suggestion



Note: All dimensions shown in micrometers (µm)

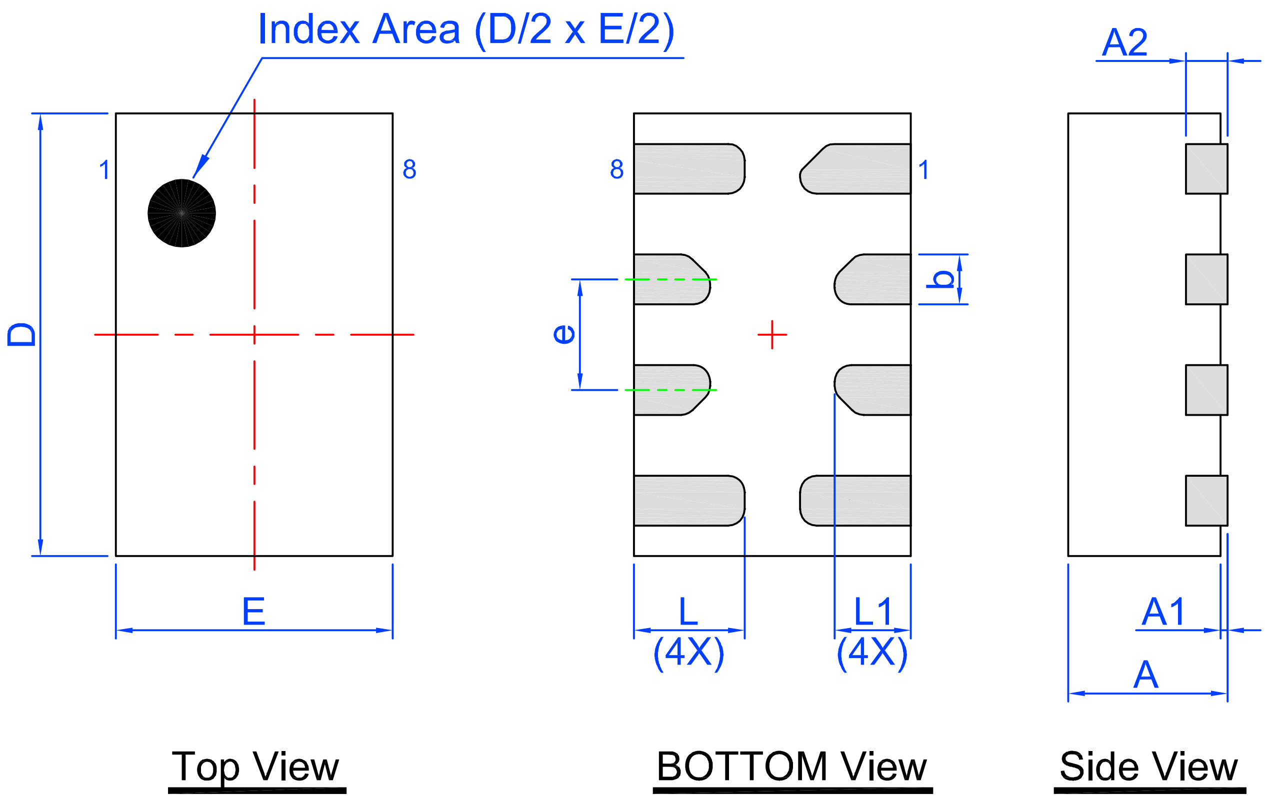
Package Top Marking System Definition



ABC - 3 alphanumeric Part Serial Number
where A, B, or C can be A-Z and 0-9

Package Drawing and Dimensions

8 Lead STDFN Package 1.0 x 1.6 mm



Unit: mm

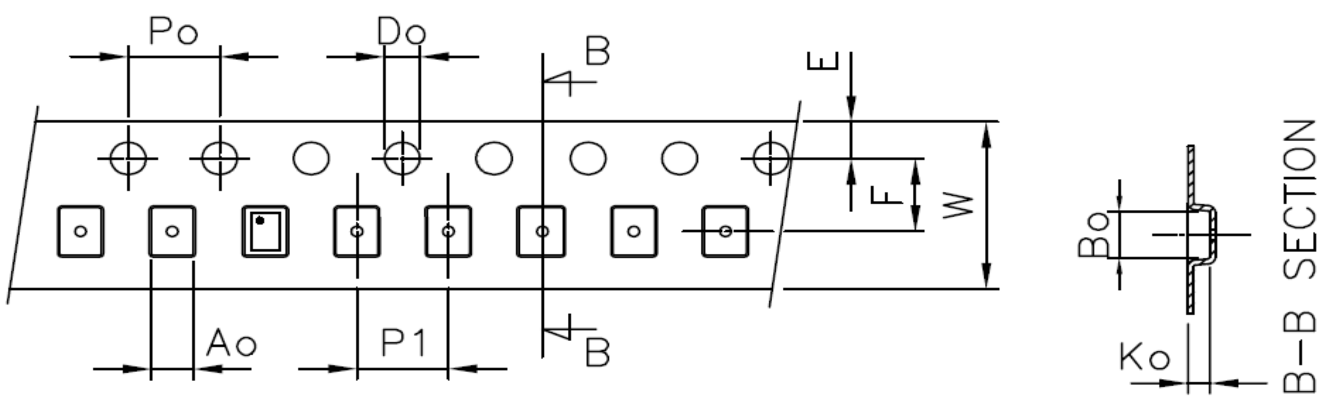
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.55	1.60	1.65
A1	0.005	-	0.050	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.13	0.18	0.23	L1	0.225	0.275	0.325
e	0.40 BSC						

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STDFN 8L 1x1.6mm 0.4P FCD Green	8	1.0 x 1.6 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	PocketBTM Length	PocketBTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STDFN 8L 1x1.6mm 0.4P FCD Green	1.12	1.72	0.7	4	4	1.55	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.88 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
8/29/2017	1.02	Updated Inrush Current Details Fixed typos
4/13/2017	1.01	Fixed Reverse Voltage Detection equation
2/23/2017	1.00	Production Release