



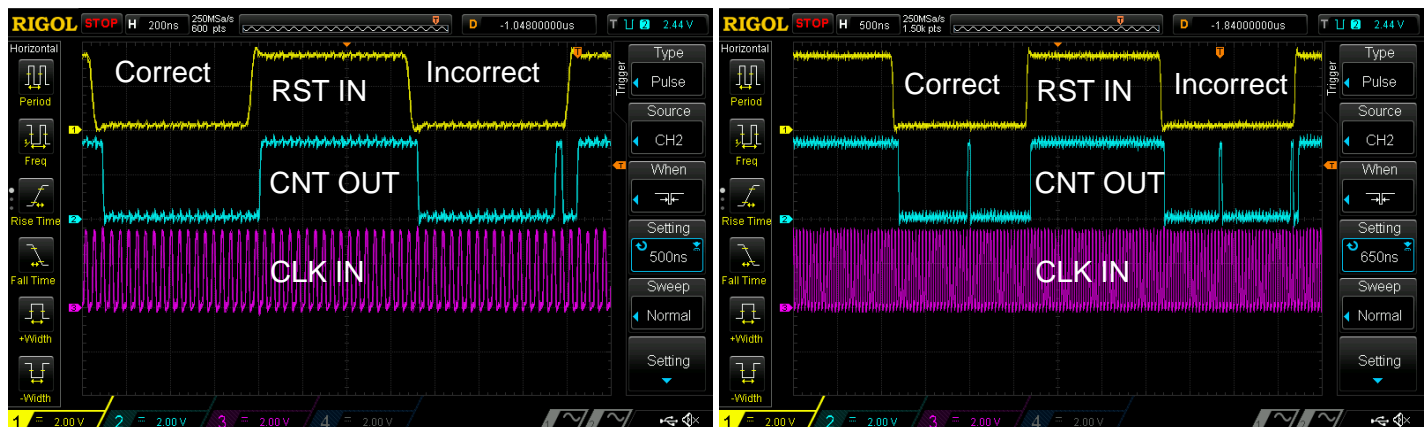
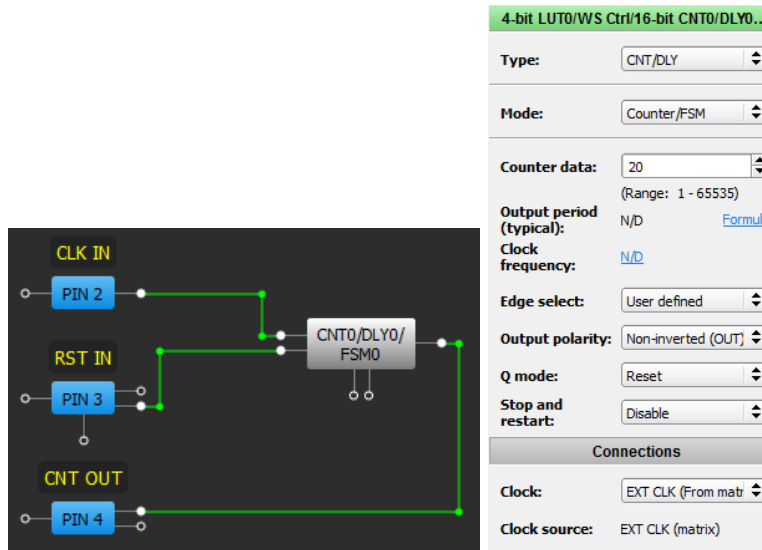
Errata disclaimer: This Errata applies to SLG46531 revision XB.

## ISSUE 1: Counter Incorrect Operation after the Reset

### Functional Block Affected: Counter

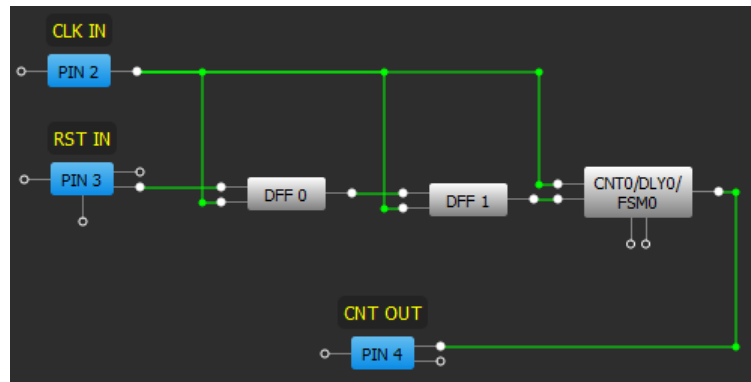
#### Description:

If the Counter Reset is asserted at the same time as a rising clock edge, it is possible that the Counter Data will be reset incorrectly and the counter output may appear faster than expected. This phenomenon appears more often as the clock frequency increases.



#### Workaround:

- Synchronize RESET input of the Counter with its CLK using 2 DFF cells as shown on picture below.

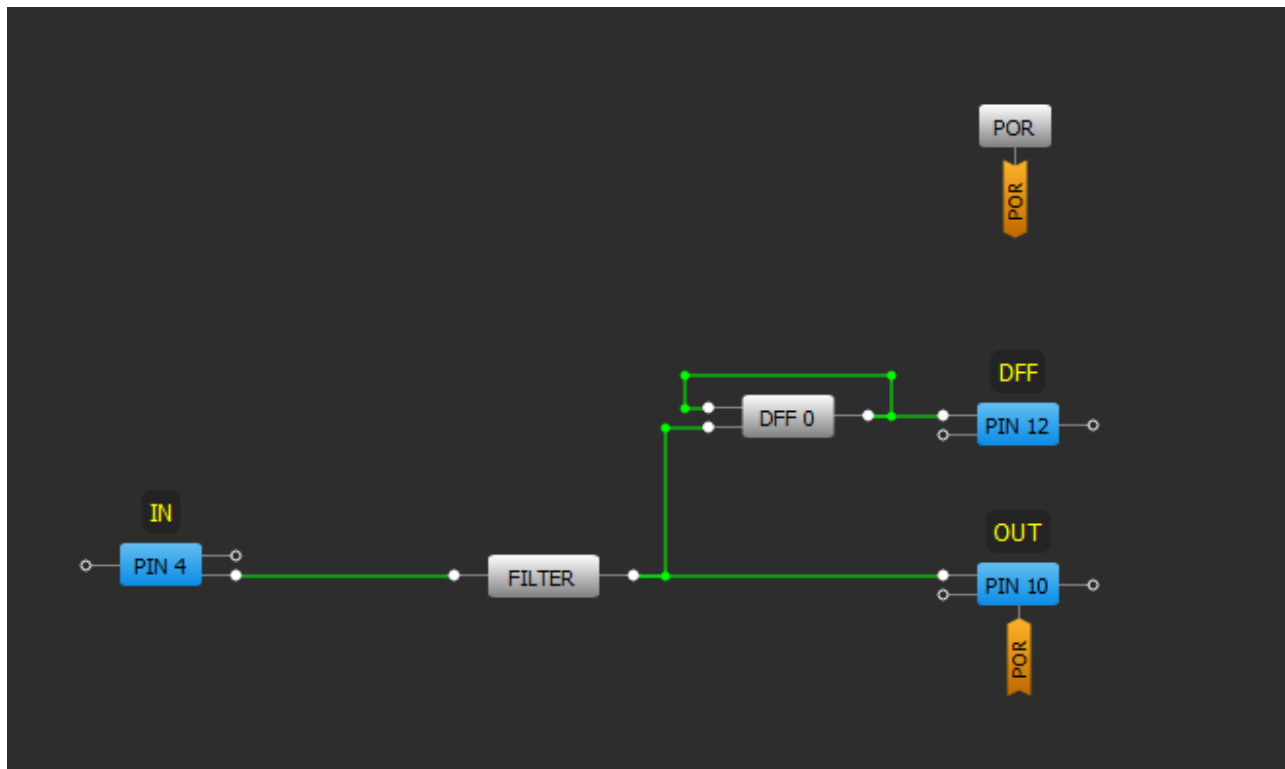


## ISSUE 2: FILTER cell does not filter out glitches

### Functional Block Affected: FILTER

#### Description:

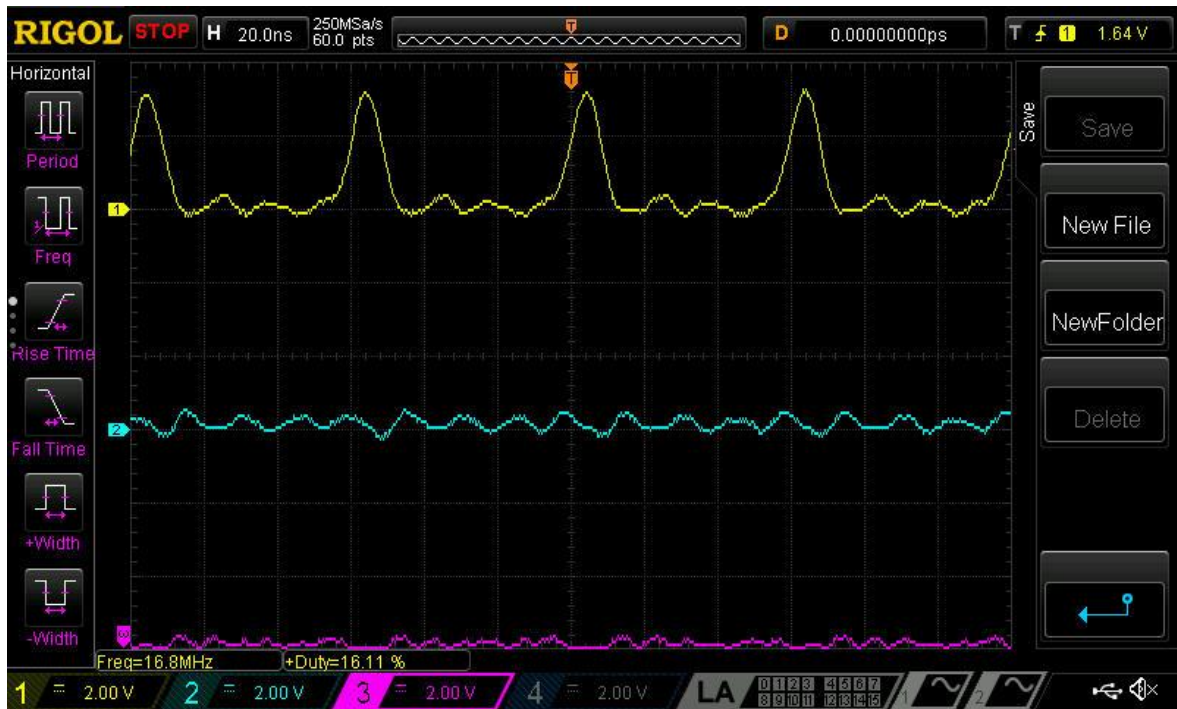
If clock type high frequency input comes in, the FILTER cell may not filter out it. There are several factors like input frequency, duty cycle and LOW duration in such signal that may lead to its passing through FILTER block.



Channel 1 (yellow/top line) – PIN#4 (IN)  
Channel 2 (light blue/2nd line) – PIN#10 (OUT)  
Channel 3 (magenta /3rd line) – PIN#12 (DFF)



1. Period is 60ns. Pulse width is 10ns DC=16.7% (Correct functionality)



2. Period is 60ns. Pulse width is 20ns DC = 33.3% (Incorrect functionality)





3. Period is 60ns. Pulse width is 30ns DC=50% (Incorrect functionality)



4. Period is 60ns. Pulse width is 40ns DC=66.67% (Correct functionality)





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Workaround:

Currently there is no workaround for this issue. Filter block is good at filtering short spontaneous glitches. It is intended to be used in series connection before the delay cell to avoid its latching (see issue #2).



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