



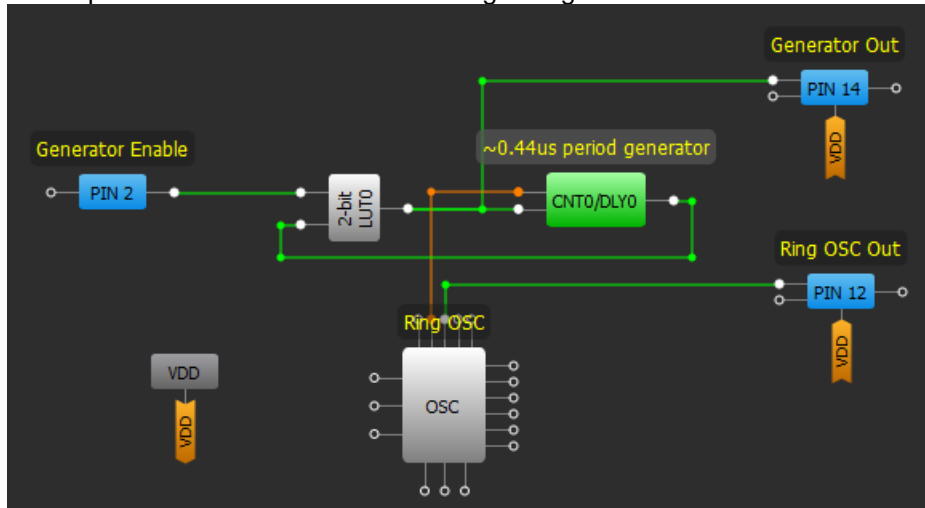
Errata disclaimer: This Errata applies to SLG46140 revision LS.

ISSUE 1: Long Ring OSC Settling Time

Functional Block Affected: Ring OSC, Delay, Counter

Description:

The Ring OSC has a longer settling time when configured as Auto Power On in the designs that have very short Ring OSC disable time. An example of such issue is in the following configuration:



| 2-bit LUT0 | | | | |
|------------|-----|-----|-----|-----|
| IN3 | IN2 | IN1 | IN0 | OUT |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |

OSC

LF OSC
RC OSC
RING OSC

Ring OSC power mode: Auto power on

Ring OSC frequency: 27.25 MHz

Ring matrix power down: Enable

Ring clock predivider by: 1

PWM & ADC clock source: RC OSC

Ring clock to matrix input: Enable

"OUT1" second divider by: 1

WS Ctrl/14-bit CNT0/DLY0

Type: CNT/DLY

Mode: Delay

Counter data: 10
(Range: 1 - 16383)

Delay time: 0.44 us [Formula](#)

Edge select: Rising

Counter value control: Reset (counter valu

DFF bypass enable: None

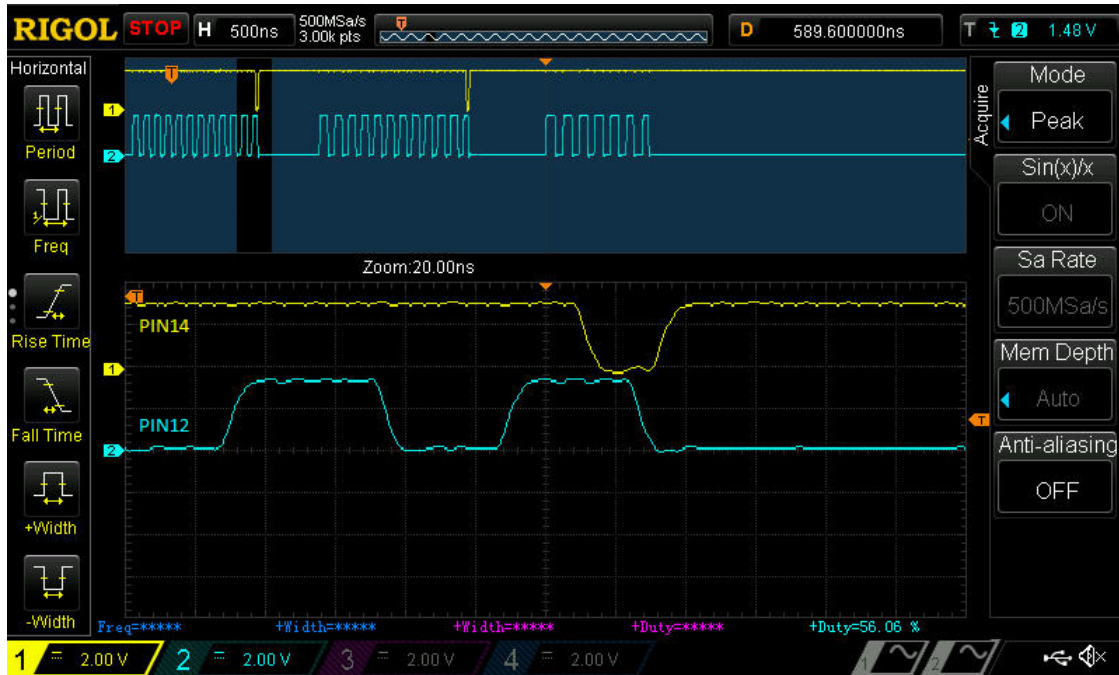
Connections

FSM data: None

Clock: Ring OSC CLK

Clock source: Ring OSC CLK Freq.

The configuration shown above generates a periodical signal with a frequency defined by the Delay cell and started by a high signal on PIN2. The issue becomes apparent in a longer settling time when the scheme generates short pulses (Delay is configured as a rising edge delay only). See waveform below.

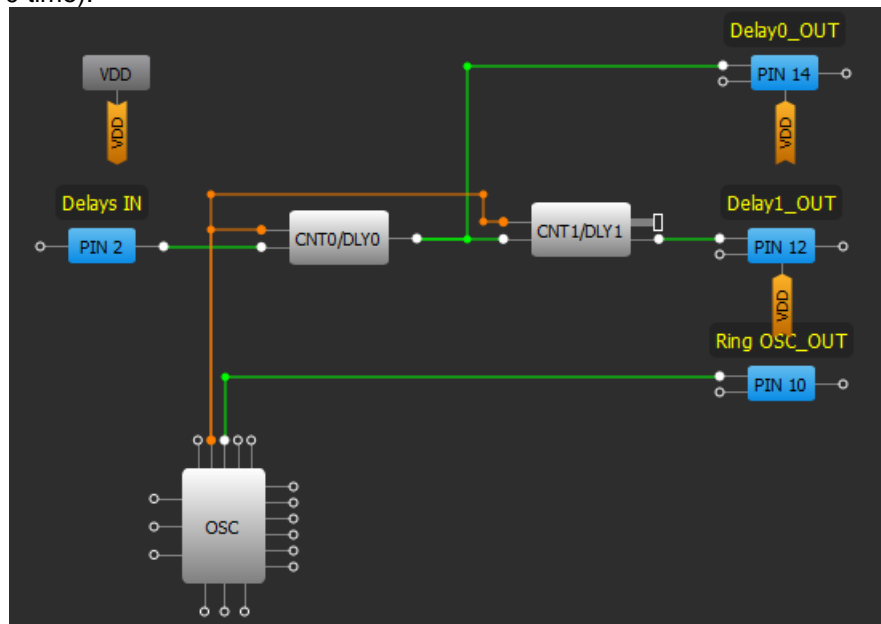


Channel 1 – 2-bit LUT0 output; Channel 2 – Ring OSC output

Such behavior will lead to substantial error in period calculations if the delay time is relatively small.

A similar situation occur while using two connected delays (all edge detect types except for a pair “Rising edge DLY – Falling edge DLY”).

In the following example, Delay0 and Delay1 are configured in the same way. However, Delay0 time is 11.4us instead of expected 0.4us (Delay0 time).





Workaround:

- Set Ring OSC power mode to “Force Power On”
- Set Turn on by register option in BG (Band Gap) block as “Enable”

ISSUE 2: PGA has an Offset when loaded

Functional Block Affected: PGA, Vref

Description:

The PGA block has an offset when its output through the VREF is loaded. For reference, shown below is the table of the load vs PGA 4x gain.

| Load, mA | Gain (ideal = 4x) |
|----------|-------------------|
| 0 | 3.87 |
| 1 | 3.84 |
| 5 | 3.78 |
| 10 | 3.71 |
| 20 | 3.5 |
| 40 | 3 |
| 80 | 2.2 |
| 160 | 1.4 |



When the load current is higher than 10 mA the output offset is large and may influence the design operation significantly.

Workaround:

- Use external buffer to support high load
-

ISSUE 3: ACMP Long Turn On Time

Functional Block Affected: ACMP

Description:

ACMPs in SLG46140 chip may have a long (up to 3.5ms at low temperatures and 1.5ms at room temperature) power up time.

Workaround:

- Use ACMPs as always powered on.
- Consider this issue in the design



SILEGO

Silego Technology

Corporate Headquarters

1515 Wyatt Drive
Santa Clara, CA 95054
USA
Phone: 408-327-8800

Silego Taiwan Office (Hsin Chu)

6F-12, Number 38, Tai Yuan Street
Tai Yuan Industrial Park, Jhubei City
Hsin Chu County, 30265, Taiwan
Phone: +886-3-560-0313
Fax: +886-3-560-0316

Silego Taiwan Office (Taipei)

9F, No.10, Ln. 321, Yangguang St,
Neihu District,
Taipei City 114, Taiwan
Phone: +886-2-2658-1038

Silego Japan Office

20F Shinjuku i-Land Tower
6-5-1 Nishi-shinjuku, Shinjuku-ku,
Tokyo 163-1320
Phone: 03-6830-5035
Fax: 03-3348-7515

Silego Korea Office

#807 Seocho Trapalace 2
1327 Seocho-Dong, Seocho-Gu
Seoul, Korea 137858
Phone: +82-3453-7560 or +82-2-3453-7127

Silego China Office (Hefei)

Rm303, Building 2, No3 TianYuan Rd
High-Tech Zone
Hefei, China 230088
Phone: +86-551-65368431
Fax: +86-551-65368432

Silego Ukraine Office

Business Center Intercity-Silego
Chervonoi Kalyny ave., 62a, 5th Floor, Room 5.1
Lviv, Ukraine
Phone: +38(032)232-80-53

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