SLG74120

Twelve Output PCI Express Clock Buffer

Features

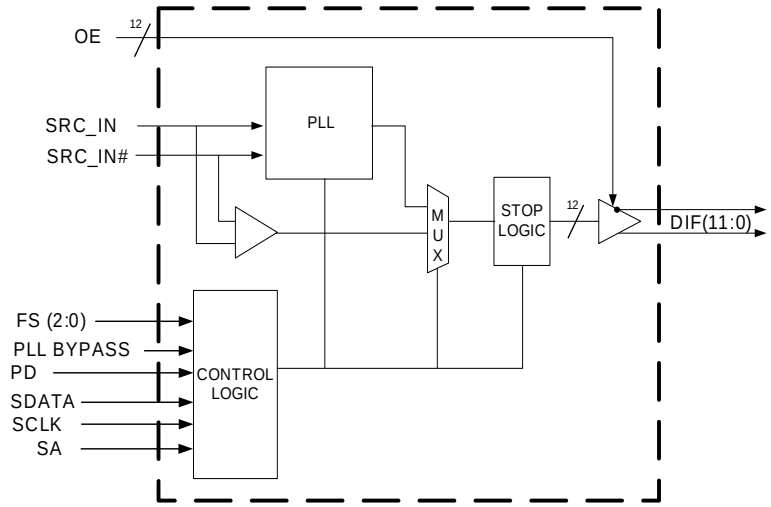
- Optimized to meet Next Generation PCI-Express Gen 2 & Gen 3 Phase Jitter
- SRC or FSB Frequency Selectable
- OE pin Control of All Outputs
- 3.3 V Supply Voltage Operation
- Output is HCSL Compatible
- SMBus Programmable Configurations
- PLL Bypass Configurable
- Programmable Bandwidth
- Glitchfree Transition Between Frequency States
- 3 Address Selection
- 64 pin TSSOP package

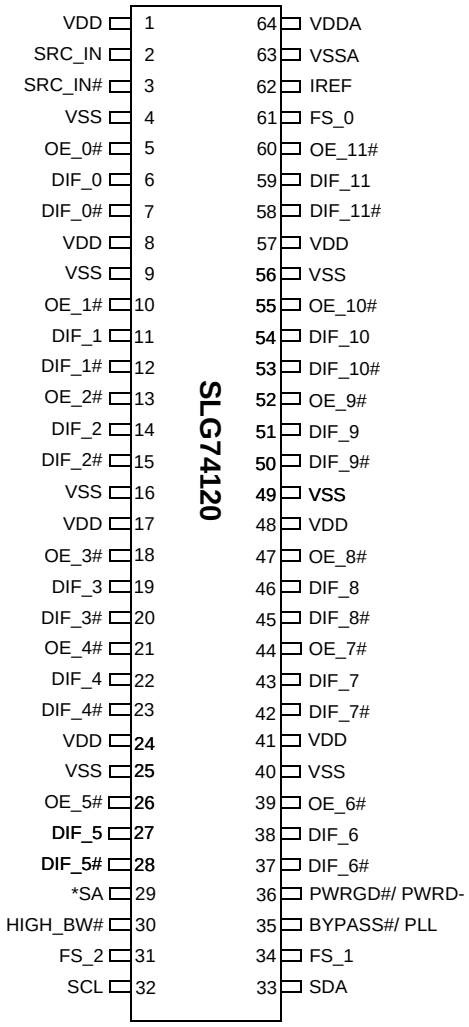
Output Summary

- DIFF SRC Clock Support
- 12 differential clock output pairs @ 0.7 V
- 50 ps O-O skew
- 50 ps Cyc_Cyc Jitter (PLL mode)
- 3.0 ps RMS phase jitter (PCIE Gen 2 Phase Jitter Compliant)
- 1.0 ps RMS phase jitter (PCIE Gen 3 Phase Jitter Compliant)

Table 1. Frequency Select Table (FS_0, FS_1, FS_2)

FS_0	FS_1	FS_2	Optimized Freq(MHz)
0	0	0	266
0	0	1	333
0	1	0	200.0
0	1	1	400
1	0	0	133
1	0	1	100
1	1	0	166
1	1	1	Hi-z





64-pin TSSOP

Note: * = contains internal pull-down resistor

Pin Description

Pin #	Name	Type	Description
1	VDD	PWR	3.3 V power supply for outputs
2	SRC_IN	I, DIF	0.7 V Differential input (eg. from CK410B clock synthesizer)
3	SRC_IN#	I, DIF	0.7 V Differential input (eg. from CK410B clock synthesizer)
4	VSS	GND	Ground for outputs
5	OE_0#	I, SE	3.3 V LVTTL active low input for enabling differential outputs(default). Controls each output pair. OE can be disabled by SMBus registers.
6	DIF_0	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
7	DIFF_0#	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
8	VDD	PWR	3.3 V power supply for outputs
9	VSS	GND	Ground for outputs
10	OE_1#	I, SE	3.3 V LVTTL active low input for enabling differential outputs(default). Controls each output pair. OE can be disabled by SMBus registers.
11	DIF_1	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
12	DIF_1#	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
13	OE_2#	I, SE	3.3 V LVTTL active low input for enabling differential outputs(default). Controls each output pair. OE can be disabled by SMBus registers.
14	DIF_2	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
15	DIF_2#	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
16	VSS	GND	Ground for outputs
17	VDD	PWR	3.3 V power supply for outputs
18	OE_3#	I, SE	3.3 V LVTTL active low input for enabling differential outputs(default). Controls each output pair. OE can be disabled by SMBus registers.
19	DIF_3	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
20	DIF_3#	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
21	OE_4#	I, SE	3.3 V LVTTL active low input for enabling differential outputs(default). Controls each output pair. OE can be disabled by SMBus registers.
22	DIF_4	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
23	DIF_4#	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
24	VDD	PWR	3.3 V power supply for outputs
25	VSS	GND	Ground for outputs
26	OE_5#	I, SE	3.3 V LVTTL active low input for enabling differential outputs(default). Controls each output pair. OE can be disabled by SMBus registers.

Pin Description (continued)

Pin #	Name	Type	Description
27	DIF_5	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
28	DIF_5#	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
29	SA	I	3.3V tolerance input. Contains internal pull-down resistor. 3.3 V LVTTL input for selecting the address. Tri-level input. Refer to the Address Selection table for Vil_SA and Vih_SA thresholds for selecting the address.
30	HIGH_BW#	I, SE	3.3 V LVTTL input for selecting the PLL bandwidth (high = low BW)
31	FS_2	I, SE	3.3 V tolerant inputs for input/output frequency selection. This can also be a GTL level, low-voltage threshold input. Refer to Table 3 2 for Vil_FS & Vih_FS thresholds.for selecting the SRC or FSB frequency.
32	SCL	I, SE	SMBus slave clock input
33	SDA	I/O, OC	Open collector SMBus data
34	FS_1	I, SE	3.3 V tolerant inputs for input/output frequency selection. This can also be a GTL level, low-voltage threshold input. Refer to Table 3 2 for Vil_FS & Vih_FS thresholds.for selecting the SRC or FSB frequency.
35	BYPASS#/PLL	I	3.3 V LVTTL input for selecting PLL or bypass mode
36	PWRGD#/PWR-DOWN		3.3 V LVTTL input to power up or power down the device
37	DIF_6#	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
38	DIF_6	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
39	OE_6#	I, SE	3.3 V LVTTL active low input for enabling differential outputs(default). Controls each output pair. OE can be disabled by SMBus registers.
40	VSS	GND	Ground for outputs
41	VDD	PWR	3.3 V power supply for outputs
42	DIF_7#	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
43	DIF_7	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
44	OE_7#	I, SE	3.3 V LVTTL active low input for enabling differential outputs(default). Controls each output pair. OE can be disabled by SMBus registers.
45	DIF_8#	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
46	DIF_8	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
47	OE_8#	I, SE	3.3 V LVTTL active low input for enabling differential outputs(default). Controls each output pair. OE can be disabled by SMBus registers.
48	VDD	PWR	3.3 V power supply for outputs
49	VSS	GND	Ground for outputs
50	DIF_9#	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.

Pin Description (continued)

Pin #	Name	Type	Description
51	DIF_9	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
52	OE_9#	I, SE	3.3 V LVTTL active low input for enabling differential outputs(default). Controls each output pair. OE can be disabled by SMBus registers.
53	DIF_10#	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
54	DIF_10	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
55	OE_10#	I, SE	3.3 V LVTTL active low input for enabling differential outputs(default). Controls each output pair. OE can be disabled by SMBus registers.
56	VSS	GND	Ground for outputs
57	VDD	PWR	3.3 V power supply for outputs
58	DIF_11#	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
59	DIF_11	O, DIF	0.7 V Differential clock outputs, that can be geared to the a ratio of the input clock. Default is 1:1.
60	OE_11#	I, SE	3.3 V LVTTL active low input for enabling differential outputs(default). Controls each output pair. OE can be disabled by SMBus registers.
61	FS_0	I, SE	3.3 V tolerant inputs for input/output frequency selection. This can also be a GTL level, low-voltage threshold input.Refer to Table 3 2 for Vil_FS & Vih_FS thresholds.for selecting the SRC or FSB frequency.
62	IREF	I	A precision resistor is attached to this pin to set the differential output current
63	VSSA	GND	Ground for PLL
64	VDDA	PWR	3.3V Power Supply for PLL

Frequency Select Pins (FS_A, FS_B, FS_C)

FS_A, FS_B, and FS_C are hardware pins, which program the appropriate output frequency of the DIF pairs. Note that the the CLK_IN frequency is equal to CLK_OUT frequency, this means that the SLG74120 is operated in the 1:1 mode only. The frequency seletction can be enabled by either FS_[2:0] hardware pins or by programing the SMBUS. The functionality is summarized in tahle below.

OE Functionality

OE# (Pin)	OE (SMBus bit)	DIFF	DIFF#	Notes
0	1	Normal	Normal	
1	0	Tristate	Tristate	
1	1	Tristate	Tristate	
0	0	Tristate	Tristate	

SA – Address Selection

SA is a hardware pin, which programs the appropriate address for the DB1200. This is a tri-level input pin that can configure the DB1200 to three different addresses (see table 3-2 for SA tri-level signal). This pin has an internal pull-down resistor, which will be a low level default at power on. The resistor values range over PVT is from 60KΩ to 170KΩ

Following are the addresses for the DB1200:

LOW = DC/DD (default using internal pull-down resistor)

MID = D6/D7

HIGH = D4/D5

Serial Bus Interface

A two-wire serial interface is provided as the programming interface for the clock synthesizer. The serial interface is fully compliance to the SMBus 2.0 specification. The registers associated with the two-wire interface initializes to their default setting upon power-up, and therefore use of this interface is optional.

The serial interface supports block write and block read operation from any SMBus master devices. For block write and block read operations, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. The block write and block read protocol is outlined in *Table 2*. The slave receiver address is 11010010 (D2h).

Table 2. Block Read and Block Write protocol

Block Write Protocol		Block Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 Bit '00000000' stands for block operation	11:18	Command Code - 8 Bit '00000000' stands for block operation
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Byte Count - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29:36	Data byte 0 - 8 bits	28	Read
37	Acknowledge from slave	29	Acknowledge from slave
38:45	Data byte 1 - 8 bits	30:37	Byte count from slave - 8 bits
46	Acknowledge from slave	38	Acknowledge
....	Data Byte N/Slave Acknowledge...	39:46	Data byte from slave - 8 bits
....	Data Byte N - 8 bits	47	Acknowledge
....	Acknowledge from slave	48:55	Data byte from slave - 8 bits
....	Stop	56	Acknowledge
		....	Data bytes from slave/Acknowledge
		....	Data byte N from slave - 8 bits
		....	Not Acknowledge
		....	Stop

Table 3. Byte Read and Byte Write protocol

Byte Write Protocol		Byte Read Protocol	
Bit	**Description**	**Bit**	**Description**
1	Start	1	Start
2:8	Slave address - 7 bits	2:8	Slave address - 7 bits
9	Write	9	Write
10	Acknowledge from slave	10	Acknowledge from slave
11:18	Command Code - 8 bits '1xxxxxxx' stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed	11:18	Command Code - 8 bits '1xxxxxxx' stands for byte operation bit[6:0] of the command code represents the offset of the byte to be accessed
19	Acknowledge from slave	19	Acknowledge from slave
20:27	Data byte - 8 bits	20	Repeat start
28	Acknowledge from slave	21:27	Slave address - 7 bits
29	Stop	28	Read
		29	Acknowledge from slave
		30:37	Data byte from slave - 8 bits
		38	Not Acknowledge
		39	Stop

Control Registers (SMBus Address = DC/DD)

Byte 0: Control Registers

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Frequency Select FS_A			RW	Latched at power up	DIF[11:0]
1	Frequency Select FS_B			RW	Latched at power up	DIF[11:0]
2	Frequency Select FS_C			RW	Latched at power up	DIF[11:0]
3	Reserved				0	
4	Reserved				0	
5	Reserved				0	
6	BYPASS# / PLL	Bypass mode	PLL mode	RW	Latched at power up	DIF[11:0]
7	HIGH_BW#	High BW	Low BW	RW	Latched at power up	DIF[11:0]

Byte 1: Output Enable Control Registers

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Output Enable DIF 0	Hi-Z	Enabled	RW	1	DIF 0, DIF 0#
1	Output Enable DIF 1	Hi-Z	Enabled	RW	1	DIF 1, DIF 1#
2	Output Enable DIF 2	Hi-Z	Enabled	RW	1	DIF 2, DIF 2#
3	Output Enable DIF 3	Hi-Z	Enabled	RW	1	DIF 3, DIF 3#
4	Output Enable DIF 4	Hi-Z	Enabled	RW	1	DIF 4, DIF 4#
5	Output Enable DIF 5	Hi-Z	Enabled	RW	1	DIF 5, DIF 5#
6	Output Enable DIF 6	Hi-Z	Enabled	RW	1	DIF 6, DIF 6#
7	Output Enable DIF 7	Hi-Z	Enabled	RW	1	DIF 7, DIF 7#

Byte 2: Output Enable Control Registers

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Output Enable DIF 8	Hi-Z	Enabled	RW	1	DIF 8, DIF 8#
1	Output Enable DIF 9	Hi-Z	Enabled	RW	1	DIF 9, DIF 9#
2	Output Enable DIF 10	Hi-Z	Enabled	RW	1	DIF 10, DIF 10#
3	Output Enable DIF 11	Hi-Z	Enabled	RW	1	DIF 11, DIF 11#
4	Reserved				0	
5	Reserved				0	
6	Reserved				0	
7	Reserved				0	

Byte 3: OE# Pin Readback Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	OE# Input DIF 0	Enabled	Hi-Z	R	Readback of the pin state	DIF 0, DIF 0#
1	OE# Input DIF 1	Enabled	Hi-Z	R	Readback of the pin state	DIF 1, DIF 1#

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
2	OE# Input DIF 2	Enabled	Hi-Z	R	Readback of the pin state	DIF 2, DIF 2#
3	OE# Input DIF 3	Enabled	Hi-Z	R	Readback of the pin state	DIF 3, DIF 3#
4	OE# Input DIF 4	Enabled	Hi-Z	R	Readback of the pin state	DIF 4, DIF 4#
5	OE# Input DIF 5	Enabled	Hi-Z	R	Readback of the pin state	DIF 5, DIF 5#
6	OE# Input DIF6	Enabled	Hi-Z	R	Readback of the pin state	DIF 6, DIF 6#
7	OE# Input DIF 7	Enabled	Hi-Z	R	Readback of the pin state	DIF 7, DIF 7#

Byte 4: OE# Pin Readback Register

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	OE# Input DIF 8	Enabled	Hi-Z	R	Readback of the pin state	DIF 8, DIF 8#
1	OE# Input DIF 9	Enabled	Hi-Z	R	Readback of the pin state	DIF 9, DIF 9#
2	OE# Input DIF 10	Enabled	Hi-Z	R	Readback of the pin state	DIF 10, DIF 10#
3	OE# Input DIF 11	Enabled	Hi-Z	R	Readback of the pin state	DIF 11, DIF 11#
4	Reserved				0	
5	Reserved				0	
6	Reserved				0	
7	Reserved				0	

Byte 5:Vendor/Revision Identification Registers

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Vendor ID Bit 0	-	-	R	0	-
1	Vendor ID Bit 1	-	-	R	1	-
2	Vendor ID Bit 2	-	-	R	1	-
3	Vendor ID Bit 3	-	-	R	0	-
4	Revision Code Bit 0	-	-	R	0	-
5	Revision Code Bit 1	-	-	R	0	-
6	Revision Code Bit 2	-	-	R	0	-
7	Revision Code Bit 3	-	-	R	0	-

Byte 6: Device ID

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	Device ID 0	-	-	R	0	-
1	Device ID 1	-	-	R	0	-
2	Device ID 2	-	-	R	1	-
3	Device ID 3	-	-	R	1	-
4	Device ID 4	-	-	R	0	-

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
5	Device ID 5	-	-	R	0	-
6	Device ID 6	-	-	R	0	-
7	Device ID 7 (MSB)	-	-	R	0	-

Byte 7: Byte Count Registers

Bit	Description	If Bit = 0	If Bit = 1	Type	Default	Output(s) Affected
0	BC0 - Writing to this register configure how many byte will be read back	-	-	RW	1	-
1	BC1 - Writing to this register configure how many byte will be read back	-	-	RW	1	-
2	BC2 - Writing to this register configure how many byte will be read back	-	-	RW	1	-
3	BC3 - Writing to this register configure how many byte will be read back	-	-	RW	0	-
4	BC4 - Writing to this register configure how many byte will be read back	-	-	RW	0	-
5	BC5 - Writing to this register configure how many byte will be read back	-	-	RW	0	-
6	BC6 - Writing to this register configure how many byte will be read back	-	-	RW	0	-
7	BC7 - Writing to this register configure how many byte will be read back	-	-	RW	0	-

Electrical Characteristics

Absolute Maximum Ratings

The table below lists the SLG74120's maximum environmental stress ratings. Functional operation at the absolute maximum and minimum is neither implied nor guaranteed. Functional operating parameters are listed in the AC and DC tables. Extended exposure to the maximum ratings may affect device reliability.

Table 3-1. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Notes
V_{DD_A}	3.3 VCore Supply Voltage	-	4.6	V	3
V_{DD}	3.3V I/O Supply Voltage	-	4.6	V	3
V_{IH}	3.3 V Input High Voltage	-	4.6	V	1,3
V_{IL}	3.3 V Input Low Voltage	-0.5	-	^{o}C	3
t_s	Storage Temperature	-65	150	V	3
ESD prot.	Input ESD protection	2000		V	2

Notes:
[1] Maximum VIH is not to exceed maximum VDD
[2] Human body model
[3] Consult technical support regarding extended operation in excess of normal DC operating parameters.

Electrical Characteristics - Clock Input Parameters

T_A = 0 to 70°C, Supply Voltage VDD = 3.3 V ± 5%

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IHDIF}	Input High Voltage-DIF_IN	Differential Inputs (single-ended measurement)	660	700	850	mV
V_{ILDIF}	Input High Voltage-DIF_IN	Differential Inputs (single-ended measurement)	-150	0.0	150	mV
V_{COM}	Input Common Mode Voltage-DIF_IN	Common Mode Input Voltage		0	V	mV
V_{SWING}	Input Amplitude-DIF_IN	Peak-to-Peak Value	510		1000	mV
dv/dt	Input Slew Rate-DIF_IN	Rise and Fall Trigger Level (175mV to 525mV)	0.5		2.0	V/ns
I_{IN}	Input Leakage Current	V_{IN} = V_{DD} =, V_{IN} = GND	-0.5		+0.5	uA
D_{TIN}	Input Duty Cycle	Measurement from differential waveform	45		55	%
J_{DIFIN_SRC}	Input Jitter - Cycle to Cycle	SRC 100MHz Output. Refer to CK410B+ Output Cycle to Cycle Jitter Spec			125	ps
J_{DIFIN_CPU}		CPU Diff Output. Refer to CK410B+ Output Cycle to Cycle Jitter Spec			50	ps

DC Electrical Characteristics

DC parameters must be sustainable under steady state (DC) conditions.

Table 3-2 DC Operating Characteristics V_{DD_A} = 3.3 V ± 5%, VDD = 3.3 V ± 5%

Symbol	Parameter	Condition	Min	Max	Units	Notes
V_{DD_A}	3.3V Core Supply Voltage	3.3V ±5%	3.135	3.465	V	
V_{DD}	3.3V I/O Supply Voltage	3.3V ±5%	3.135	3.465	V	
V_{IH}	3.3V Input High Voltage	V_{DD}	2.0	V_{DD}+0.3	V	
V_{IL}	3.3V Input Low Voltage		V_{SS}-0.3	0.8	V	
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{DD}$	-5	+5	µA	
V_{IH_FS}	3.3V Input High Voltage	V_{DD}	0.7	V_{DD}-0.3	V	3
V_{IL_FS}	3.3 Input Low Voltage		V_{SS}-0.3	0.35	V	3
V_{IL_SA}	3.3 Input Low Voltage		0	0.9	V	
V_{IM_SA}	3.3V Input Medium Voltage		1.3	2.0	V	
V_{IH_SA}	3.3V Input High Voltage		2.4	V_{DD}	V	
V_{OH}	3.3V Output High Voltage	I_{OH} = -1mA	2.4		V	1
V_{OL}	3.3V Output Low Voltage	I_{OL} = 1mA		0.4	V	1
C_{IN}	Input Capacitance		2.5	4.5	pF	4
C_{OUT}	Output Capacitance		2.5	4.5	pF	4
L_{PIN}	Pin Inductance			7	nH	
ta	Ambient Temperature	No Airflow	0	70	^{o}C	

[1] Signal edge is required to be monotonic when transitioning through this region
[2] Input Leakage Current does not include inputs with pull-up or pull-down resistors. Inputs with resistors should state current requirements.
[3] Internal voltage reference is to be used to guarantee Vih_FS and Vil_FS thresholds levels over devices full operating range
[4] Ccomp capacitance based on pad metallization and silicon device capacitance. Not including pin capacitance

Power Management

The values below are estimates for the power specifications.

Table 3-3. Maximum Allowed Current

Condition	Max 3.3V Supply Consumption Max Discrete Cap Loads V_{DD} = 3.465 V All Static Inputs - V_{DD} or V_{SS}
Powerdown Mode (VTT_PWRGD# / PWRDWN = 1)	All Pairs Tristated = 24mA
Full Active	375 mA

Skew and Jitter Characteristics

Skew and jitter characteristics are critical output timing parameters affecting downstream receivers of the clocking signals.

Table 3-4. Output Relational Timing Parameters

Electrical Characteristics - Skew and Differential Jitter Parameters					
T_A = 0 - 70^{o}C					
Group	Description	min	max	units	notes
CLK_IN, DIFF[x:0]	Input-to-Output Delay in PLL mode (1:1 only), nominal value	-250	250	ps	1,2,3,4,5

Electrical Characteristics - Skew and Differential Jitter Parameters					
T_A = 0 - 70°C					
CLK_IN, DIF[x:0]	Input-to-Output Delay in Bypass mode (1:1 only), nominal vlaue	2.5	4.5	ns	2,3,4
DIF[11:0]	Output-to-Output Skew across all 12 outputs (Common to Bypass and PLL mode - all outpus at same gear	0	50	ps	1,2,3
DIF[11:0]	Differential Phase Jitter (RMS Value)		10	ps	1,4,6
DIF[11:0]	Differential Spread Spectrum Tracking Error (peak to peak)		100	ps	1,4,7

[1] Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.
[2] Measured from differential cross-point to differential cross-point
[3] All Bypass Mode Input-to-Output specs refer to the timing between an input edge and the specific output edge created by it.
[4] This parameter is deterministic for a given device
[5] Measured with scope averaging on to find mean value.
[6] This parameter is measured at the outputs of two separate SLG74120 devices driven by a single CK410B. The SLG74120's must be set to high bandwidth. Differential phase jitter is the accumulation of the phase jitter not shared by the outputs (e.g. not including the affects of spread spectrum). Target ranges of consideration are agents with BW of 1-22 MHz and 11-33 MHz.
[7] Differential spread spectrum tracking error is the difference in spread spectrum tracking between two SLG74120 devices This parameter is measured at the outputs of two separate SLG74120 devices driven by a single CK410B in Spread Spectrum mode. The SLG74120's must be set to high bandwidth. The spread spectrum characteristics are: maximum of 0.5%, 30-33 kHz modulation frequency, linear profile.

Table 3-5. PLL Bandwidth, Peaking and Phase Jitter Impact

Group	Parameter	Target	Min	Max	Notes
DIF	PLL Jitter Peaking (HIGH_BW# = 0)	<1 dB	---	<2.5 dB	2
DIF	PLL Jitter Peaking (HIGH_BW# = 1)	<1 dB	---	<2.0 dB	2
DIF	PLL Bandwidth (HIGH_BW# = 0)	3 MHz	2 MHz	4 MHz	1
DIF	PLL Bandwidth (HIGH_BW# = 1)	1 MHz	700 kHz	1.4 MHz	1
DIF	Output phase jitter impact - PCIe* Gen1 (including PLL BW 1.5-22 MHz)		0ps	108 ps	3, 6
DIF	Output phase jitter impact - FBD (including PLL BW 11-33 MHz)		0 ps	3 ps RMS	3, 4
DIF	Output phase jitter impact - PCIe Gen2 (including PLL BW 8-16 MHz		0 ps	3.1 ps RMS	3, 5
DIF	Output phase jitter impact - PCIe Gen3 (including PLL BW 2-4 MHz		0 ps	1.0 ps RMS	3, 5

NOTES:
[1] Measured at 3 db down or half power point .
[2] Measured as maximum pass band gain. At frequencies within the loop BW, highest point of magnification is called PLL jitter peaking.
[3] Post processed evaluation through Intel supplied Matlab scripts.
[4] Refer to FB-DIMM Specification: “High Speed Differential Point-to-Point Link at 1.5 V” for updates to this specification.
[5] PCIe* filter characteristics are subject to final ratification by PCISIG Please check the PCI* SIG for the latest specification. Tested with SLG74120 driven by low phase noise signal generator such as an Agilent 8133A.
[6] These jitter numbers are defined for a BER of 1E-12. Measured numbers at a smaller sample size have to be extrapolated to this BER target.

DIF Output Timing Characteristics (Non SSC Clock Input)

Table 3-6. DIF 0.7 V AC Timing Characteristics (Non-Spread Spectrum Mode)

Symbol	Parameter	CLK 100 MHz, 133 MHz, 166 MHz, 200 MHz, 266 MHz, 333 MHz, 400 MHz		Unit	Notes
		Min	Max		
Tstab	Clock Stabilization Time		1.8	ms	22
Laccuracy	Long Accuracy		0	ppm	4,8,16
Tperiod	Average Period	-0.3%	+0.3%	ns	4,5,8
Tabsmin	Absolute Minimum Host CLK Period	-2.5%		ns	4,5,8
Trise	Rise Time	175	700	ps	2,4,7
Edge_rate	Edge_rate	0.5	2.0	V/ns	2,4,7
ΔTrise	Rise Time Variation		125	ps	4,7,18
ΔTfall	Fall Time Variation		125	ps	4,7,18
Rise/Fall Matching			20%		4,7,19,21
Vhigh	Voltage High (typ. 0.70 Volts)	660	850	mV	4,7,10
Vlow	Voltage Low (typ. 0.0 Volts)	-150		mV	4,7,11
Vcross absolute	Absolute Crossing Point Voltages	250	550	mV	1,3,4,7,14
Vcross relative	Relative Crossing Point Voltages	Calc	Calc		4,6,7,14
Total Δ Vcross	Total Variation of Vcross Over All Edges		140	mV	4,7,15
Tccjitter	Cycle-to-Cycle Jitter		50	ps	4,8,20
Duty Cycle		45	55	%	4,8
Vovs	Maximum Voltage (Overshoot)		$V_{high + 0.3V}$		4,7,12
Vuds	Maximum Voltage (Undershoot)		$V_{low - 0.3V}$		4,7,13
Vrb	Ringback Voltage	0.2	N/A	Volt	4,7

[1] Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLK#

[2] Measured from Vol = 0.175 V to Voh = 0.525 V. Only valid for Rising clock and Falling Clock#. Signal must be monotonic through the Vol to Voh region for Trise and Tfall

[3] This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing

[4] Test configuration is Rs=33.2 O, Rp=49.9, 2 pF

[5] The average period over any 1 µs period of time must be greater than the minimum and less than the maximum specified period

[6] Vcross(rel) Min and Max are derived using the following, Vcross(rel) Min = 0.250 + 0.5 (Vhavg - 0.700),

Vcross(rel) Max = 0.550 - 0.5 (0.700 – Vhavg), (see Figure 3 4 for further clarification)

[7] Measurement taken from Single Ended waveform

[8] Measurement taken from differential waveform

[9] Unless otherwise noted, all specifications in this table apply to all processor frequencies

[10] VHigh is defined as the statistical average High value as obtained by using the Oscilloscope VHigh Math function

[11] VLow is defined as the statistical average Low value as obtained by using the Oscilloscope VLow Math function

[12] Overshoot is defined as the absolute value of the maximum voltage

[13] Undershoot is defined as the absolute value of the minimum voltage

[14] The crossing point must meet the absolute and relative crossing point specifications simultaneously

[15] ΔVcross is defined as the total variation of all crossing voltages of Rising CLOCK and Falling CLOCK#. This is the maximum allowed variance in Vcross for any particular system

[16] Using frequency counter with the measurement interval equal or greater than 0.15 s, target frequencies are 100,000,000 Hz, 133,333,333 Hz, 166,666,666 Hz and 200,000,000 Hz

[17] Using frequency counter with the measurement interval equal or greater than 0.15 s, target frequencies are 99,750,00 Hz, 133,000,000 Hz, 166,250,000 Hz and 199,500,000 Hz

[18] Measured with oscilloscope, averaging off, using min max statistics. Variation is the delta between min and max.

[19] Measured with oscilloscope, averaging on, The difference between the rising edge rate (average) of clock verses the falling edge rate (average) of clock#

[20] Measured with device in PLL mode, in BYPASS# mode jitter is additive

[21] Rise/Fall matching is derived using the following, 2*(Trise – Tfall) / (Trise + Tfall)

[22] This is the time from the assertion of the VTT_PWRGD# pin or the ramping of the power supply or the time from valid Clk_IN input clocks until the time that stable clocks are output from the buffer chip (PLL locked).

Input Edge Rate

Input edge rate is based on single ended measurement. This is the minimum input edge rate at which the SLG74120 devices are guaranteed to meet all performance specifications. The edge rate is subjected to process change or design change on the clock components.

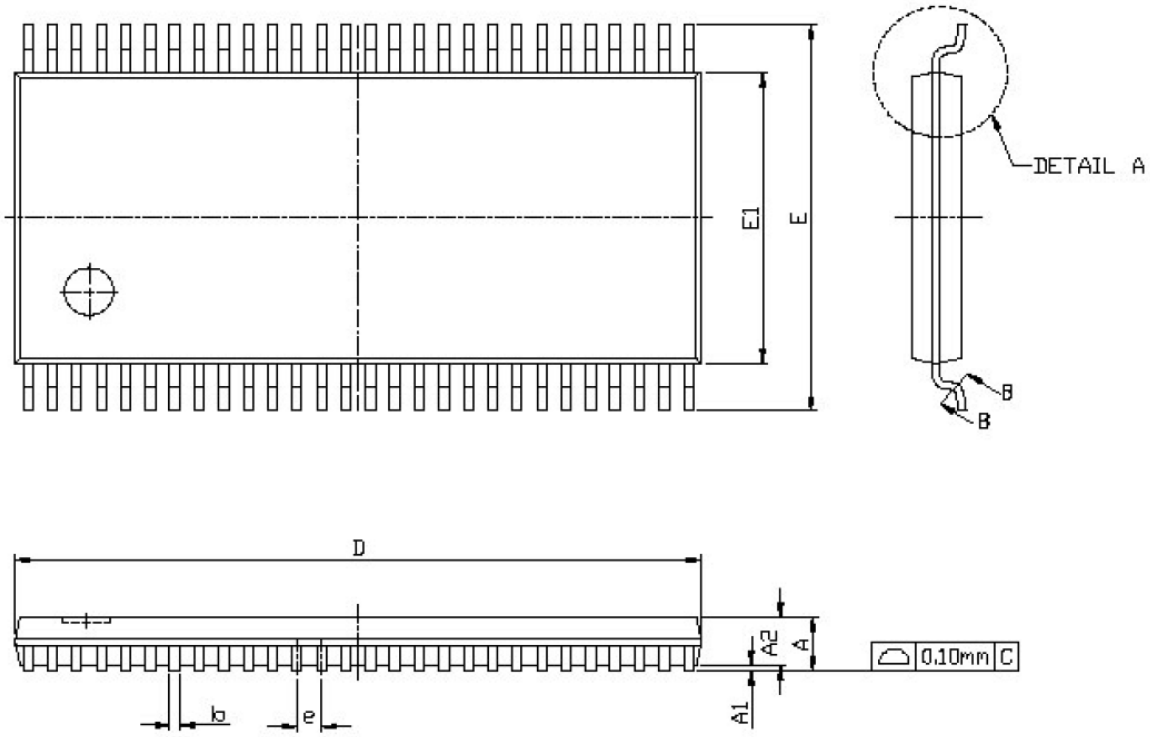
Frequency	Min	Max	Unit
100 MHz	0.35	N/A	V/ns
133 MHz	0.35	N/A	V/ns
166 MHz	0.35	N/A	V/ns
200 MHz	0.35	N/A	V/ns
266 MHz	0.40	N/A	V/ns
333 MHz	0.40	N/A	V/ns
400 MHz	0.40	N/A	V/ns

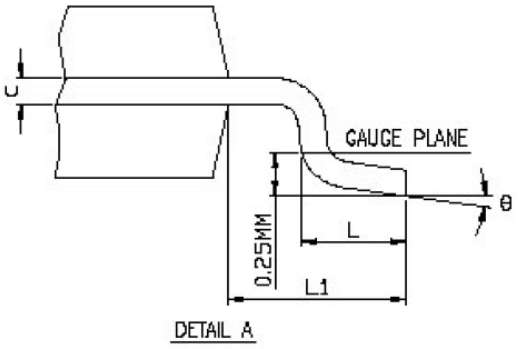
Ordering Information

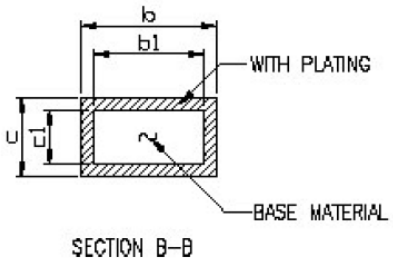
SLG74120T	64 Lead Green Package TSSOP	Commercial, 0° to 70°C
SLG74120TTR	64 Lead Green Package TSSOP - Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

64 Lead TSSOP Package







SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A			1.20			0.047
A1	0.05		0.15	0.002		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
E	8.00	8.10	8.20	0.315	0.319	0.323
E1	6.00	6.10	6.20	0.236	0.240	0.244
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF.			0.039 REF.		
b	0.20 TYP.			0.008 TYP.		
⚠ b1	0.15 TYP.			0.006 TYP.		
c	0.09		0.20	0.004		0.008
⚠ c1	0.05	0.15	0.16	0.002		0.006
e	0.50 BSC.			0.020 BSC.		
θ	0		8	0		8

	D (MM)			JEDEC
N	MIN.	NOM	MAX.	
48	12.40	12.50	12.60	MO-153ED
56	13.90	14.00	14.10	MO-153EE
64	16.90	17.00	17.10	MO-153EF

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Hub & Reel Size (mm)	Trailer A		Leader B		Pocket Tape (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
TSSOP 64L 240 mil Green	64	17x8.1	2,000	2,000	330/100	42	504	42	504	24	12

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
TSSOP 64L 240 mil Green	8.4	17.3	1.6	4	12	1.5	1.75	11.5	24