# SLG55031

## GreenFET™ High Voltage Gate Driver

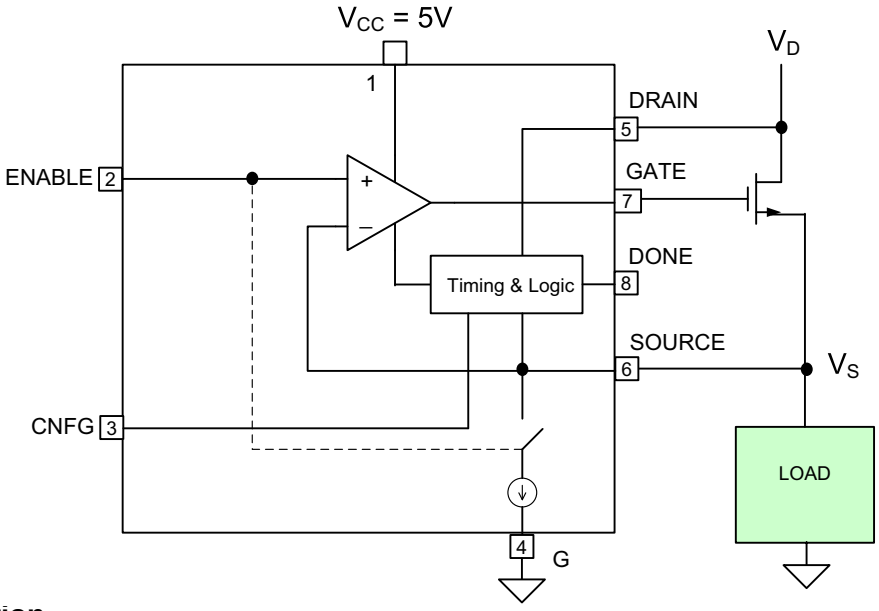
### Features

- Drain Voltage Range 0.7V to 1.5V
- Controlled Load Discharge Rate
- Controlled Turn on Slew Rate
- Pb-Free / RoHS compliant
- Halogen-Free
- 2mm x 2mm TDFN-8 Package

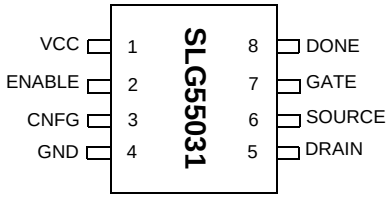
### Applications

- Low Transient Load Switching
- Personal computers and Servers
- Hot Plugging Applications
- Power Rail Switches

### Block Diagram




### Pin Configuration




**TDFN-8**

### Overview

The SLG55031 N-Channel FET Gate Driver is used for controlling the ramping slew rate of the source voltage on N-Channel FET switches from a CMOS logic level input. Intended as supporting control elements for switched voltage rails in energy efficient advanced power management systems, these devices also include circuits to discharge opened switched voltage rails. SLG55031 uses an external resistor connected between the CNFG pin and GND to establish the slew rate. F

SLG55031 ramps $V_S$ from 10% to 90% of 1.50V in 33µs with External Resistor = 560kΩ

## Pin Description

| Pin Name | Pin Number | Type | Pin Description |
|---|---|---|---|
| VCC | 1 | Power | Supply Voltage 5V |
| ENABLE | 2 | Input | CMOS Logic Level. High True for SLG55031 and SLG5AP033. Low True for SLG5AP032 |
| CNFG | 3 | Input | Resistor or Capacitor Connection for timing configuration |
| GND | 4 | GND | Ground. |
| DRAIN | 5 | Input | FET Drain Connection |
| SOURCE | 6 | Input | Source Connection |
| GATE | 7 | Output | FET Gate Drive |
| DONE | 8 | Output | Output CMOS Open Drain - Power Good, indicates external FET fully on. |

## Ordering Information

| Part Number | External Timing Component | Enable Polarity | External FET Threshold Voltage Range | Package Type |
|---|---|---|---|---|
| SLG55031VTR | External Resistor | HIGH True Active | 1.5V < VT < 2.5V | TDFN-8 - Tape and Reel (3k units) |

## Absolute Maximum Conditions

| Parameter | Min. | Max. | Unit |
|---|---|---|---|
| $V_{CC}$to GND | -0.3 | 6.0 | V |
| Voltage at Logic Input pins | -0.3 | 6.0 | V |
| Current at input pin | -1.0 | 1.0 | mA |
| Storage temperature range | -65 | 150 | °C |
| Operating temperature range | 0 | 70 | °C |
| Junction temperature | -- | 150 | °C |
| Moisture Sensitivity Level | 1 | | |

## Electrical Characteristics (-10°C to 75°C)

| Symbol | Parameter | Condition/Note | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 4.75 | 5.0 | 5.25 | V |
| $I_q$ | Quiescent Current | ENABLE = 1, $V_G$ not ramping | | 1.5 | 5 | µA |
| $I_{STBY}$ | Standby Current | ENABLE = 0 | | 2 | 3 | µA |
| T | Operating Temperature | | 0 | 25 | 70 | °C |
| $V_D$ | Driven FET Drain Voltage | May dynamically vary | 0.7 | -- | 1.5 | V |
| $V_G$ | Gate Voltage | Tracks Supply $V_{CC}$ | 4.75 | 5.0 | 5.25 | V |
| $T_{VT}$ | FET Turn on Delay | FET VT <2.0V<br>FET GATE CIN < 4nF | 3 | 8 | -- | µs |
| $I_{DISCHARGE}$ | Internal Discharge Equiva-lent Current | Discharges MOSFET Source | -- | -- | 10 | mA |
| $V_{IH}$ | HIGH-level input voltage | ENABLE pin | 2.0 | -- | -- | V |
| $V_{IL}$ | LOW-level Input voltage | ENABLE pin | -- | -- | 1.0 | V |
| $I_{IH}$ | HIGH-level Input Current | Digital pins, $V_{IN} = V_{CC}$ | -1.0 | -- | 1.0 | µA |
| $I_{IL}$ | LOW-level input Current | Digital pins, $V_{IN}$ = 0V | -1.0 | -- | 1.0 | µA |
| $V_{OH\_LOGIC}$ | DONE Pull-up Voltage | Open Drain Output Buffer | -- | -- | 5.5 | V |

## Description

In a typical application, de-asserting ENABLE turns off the external power N-FET. The voltage at the load is discharged through the discharge control path internal to the SLG55031. The rate of discharge is current limited to 10ma.

When ENABLE is asserted, gate voltage is applied to the gate of the external power N-FET within 10µs (typical) then the gate voltage is ramped up to $V_{CC}$ - $V_D$ (3.5V typical) at a slew rate determined by the value of the external resistor or capacitor connected to the CNFG pin of the SLG55031. Monotonic rise of the external FET's source voltage $V_S$ is maintained even as Source current increases after the load device turn on threshold voltage is reached. After the Source voltage has ramped up to the Drain Voltage – the voltage drop contribution by $R_{DS-ON}$ of the FET, the external FET is fully on and the open drain DONE signal is asserted.

If a voltage is not present on the Drain Sense Pin prior to assertion of ENABLE, the FET's gate will be immediately driven high turning the FET fully on.

DONE may be used as the ENABLE control of a second SLG5AP03X connected in series thereby providing power on sequence control of a number of switched power rails, or used in a 'wired and' with other DONE signals to indicate all switched power rails are in a power good condition.

## Configuration Options

The SLG55031 is configured with external passive devices to select between two widely separate ramp slew rates. See the following Table for details

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## Configuration Pin Usage Table

| Resistor to Ground (SLG55031) to 1.5V Rail | | | |
|---|---|---|---|
| Value (Ω) | 400K | 560K | 750K |
| Typical Slew Time (µs) | 23 | 33 | 45 |

## Timing Diagram - Initial P-ON

$V_{CC}$ to the SLG55031 must reach $V_{CC}$ min (4.75V) before the device will begin to be operational. ENABLE[1] must be asserted 100µs after 100% of $V_{CC}$ has been attained. If V_DRAIN is present at a minimum of 3µs prior to assertion of the ENABLE, the Source will begin to ramp towards V_DRAIN after T_VT (10µs typically), the time required for the gate of the FET to be past turn on threshold (typically 2.0V). Carefully examine specific FET turn-on threshold as well as FET C-IN and if the values fall outside of the range of values covered in the electrical specifications section of this document, consult Silego for applications assistance in determining the value of T_VT.

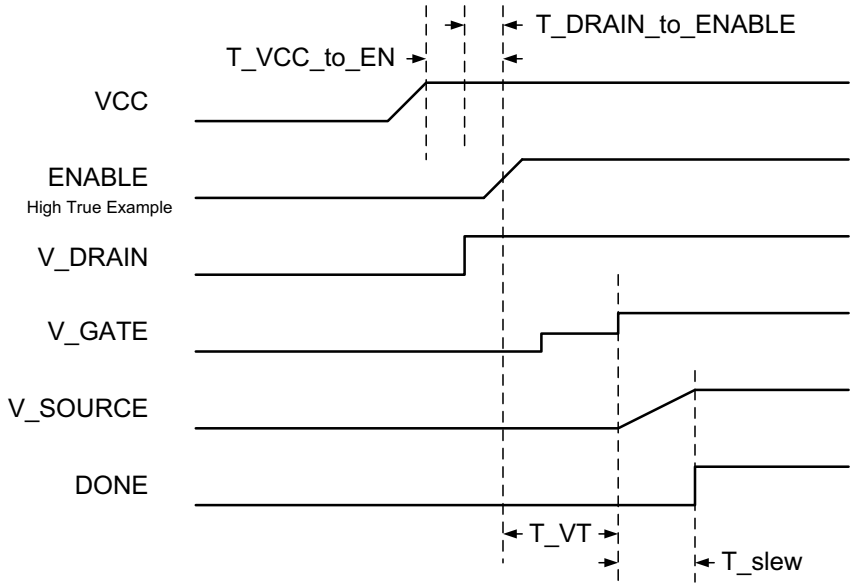



**Diagram 1 Enable after VCC**

If V_DRAIN is not present prior to the assertion ENABLE, the driven FET will be turned on immediately following assertion of ENABLE and subsequent application of a voltage on the Drain of the FET will be directly applied to the Source (Diagram 2). Again, $V_{CC}$ must have reached $V_{CC-MIN}$ before ENABLE will operate the device. V_Gate will be pulled to $V_{CC}$ after which the V_Source will track the voltage applied to the Drain of the FET.

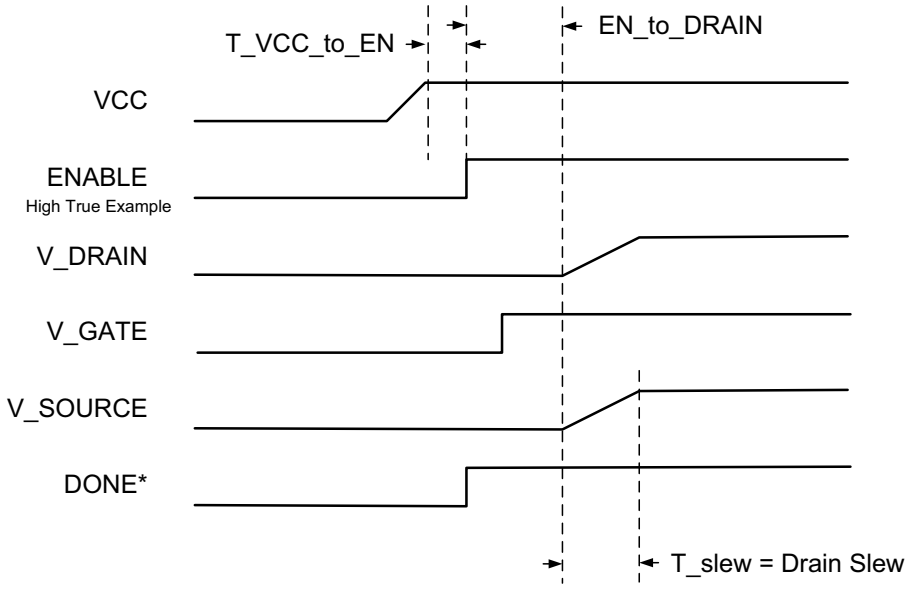



**Diagram 2**

*1 T_$V_{CC}$ to ENABLE = 100µs assertion delay (when $V_{CC}$ initially ramping up to 100% of $V_{CC}$).*
*2 Enable assertion transition time must be less than 1µs.*
** If V_Drain = 0V prior to assertion of ENABLE, DONE becomes true co-incident with assertion of ENABLE.*
** In the case of V_DRAIN after ENABLE, the definition of Arrival and Ramp Time are not valid*

## Timing Diagram - Rail Switching

The two components of the FET turn-on time consist of the time it takes to drive the FET's gate up to turn-on threshold (T_VT) added to the time it takes for the FET's source voltage to ramp (T_Slew) up fully on into the driven load. The timing diagram and table below show the min/max values for these two components vs. different rail source voltage. The T_VT delay is 8µs - 10µs typically (with FET VT = 2.0V) depending on the threshold voltage of the FET being driven (Diagram 3).

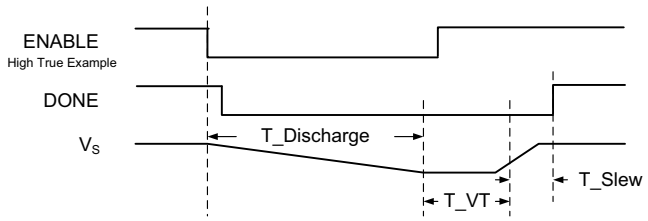



**Diagram 3**

The Table below and Diagram 3 illustrate source voltage ramp times for various slew rates and resulting total turn on time (ENABLE to DONE) when using the SLG55031 for several selected ranges of drain voltages..

| | Min (µSec) | Typ (µSec) | | Max (µSec) |
|---|---|---|---|---|
| **SLG55031** | | | | |
| **R_ext = 560KΩ** | **V_Drain Voltage (FET VT = 1.5V to 2.5V)** | | | |
| | | **1.35V** | **1.50V** | |
| T_Slew* | 20 | 30 | 33 | |
| T_DONE** | | 42 | 46 | 65 |
| Recommended FET: ON Semi NTMFS4834N | | | | |
| | | | | |

(See Diagram 4 below for more details)
* T_Slew: As V_Source increases from 10% to 90% of V_Drainl; e.g. ramp time
** T_Done: From assertion of Enable to V_Source = 90% of V_Drain; e.g. arrival time

## Timing Definition of Arrival Time and Ramp Time

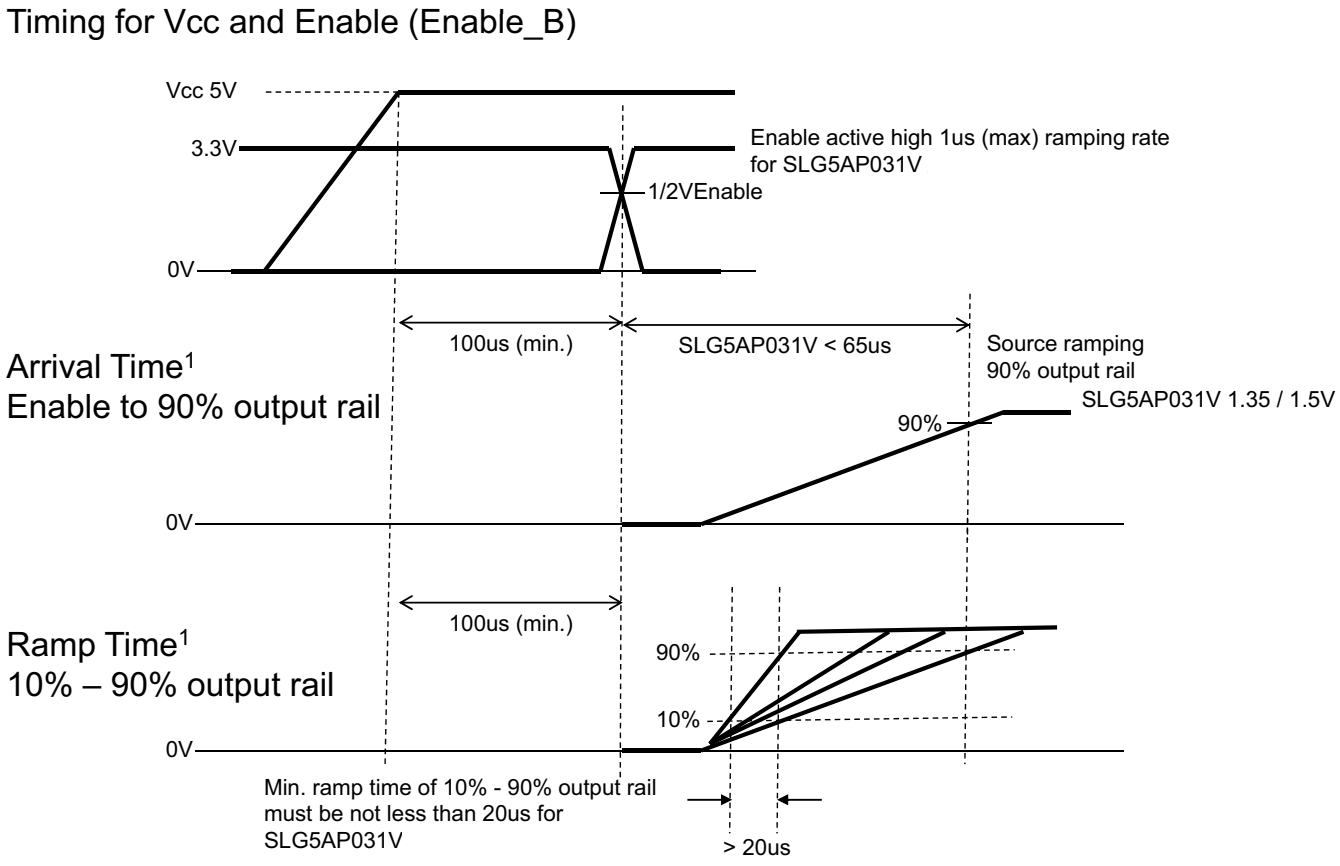
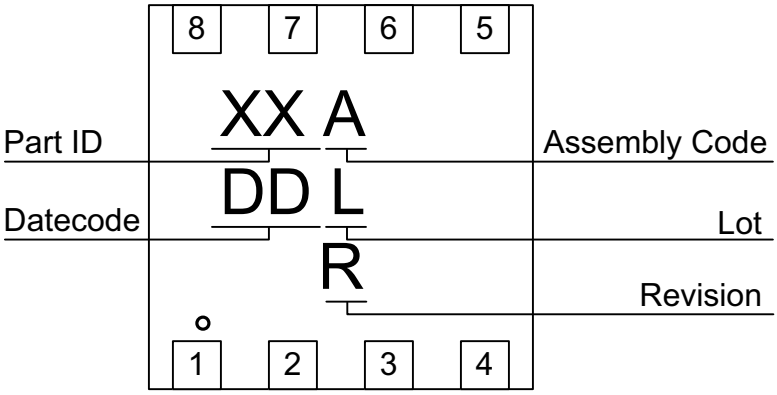



**Diagram 4**

*1 The definition of Arrival Time and Ramp Time is only valid for ENABLE (asserted with a 100µs delay) after $V_{CC}$ has reached 100% and V_DRAIN is present prior to assertion of ENABLE*

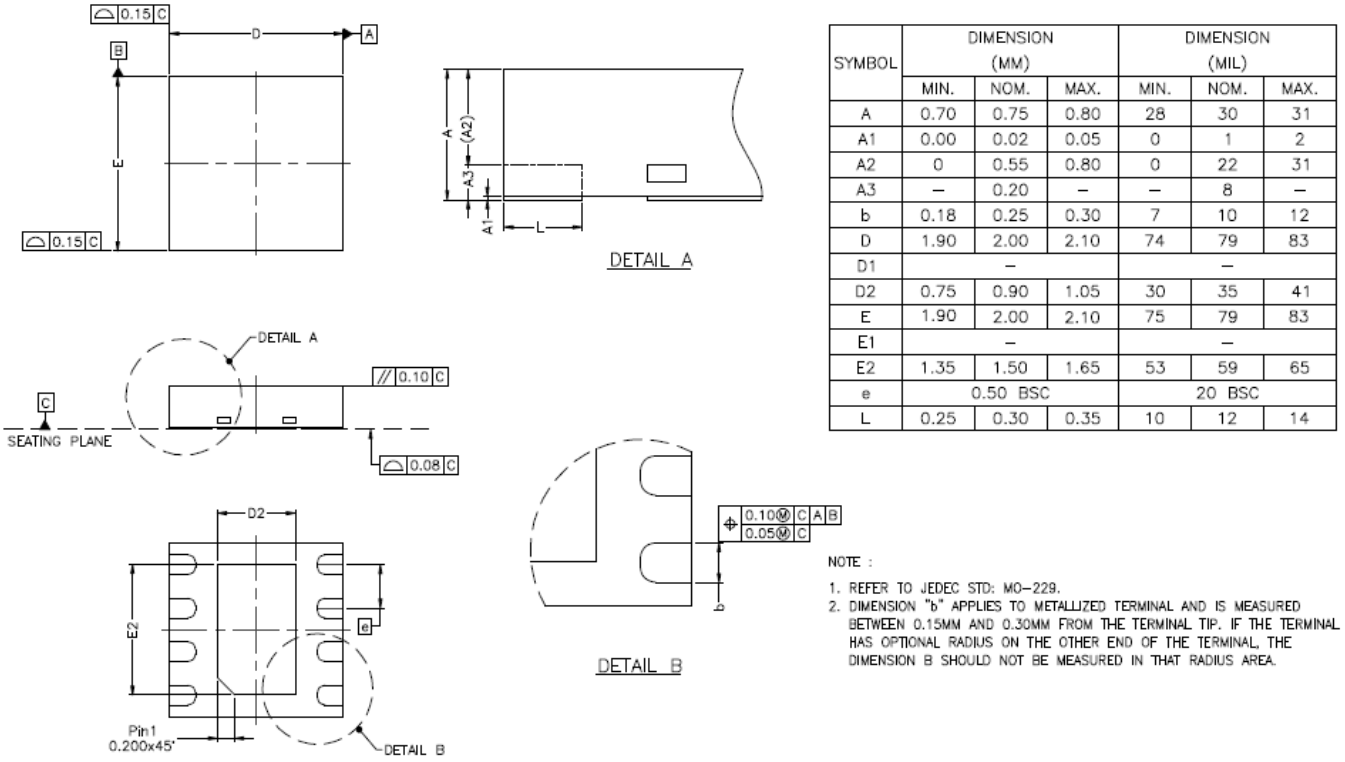
## Package Top Marking System Definition




XX – Part ID Field: identifies the specific device configuration
A – Assembly Code Field: Assembly Location of the device.
DD – Date Code Field: Coded date of manufacture
L – Lot Code: Designates Lot #
R – Revision Code: Device Revision

## Package Drawing and Dimensions

**8 Lead TDFN Package**




| SYMBOL | DIMENSION (MM) | | | DIMENSION (MIL) | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 28 | 30 | 31 |
| A1 | 0.00 | 0.02 | 0.05 | 0 | 1 | 2 |
| A2 | 0 | 0.55 | 0.80 | 0 | 22 | 31 |
| A3 | – | 0.20 | – | – | 8 | – |
| b | 0.18 | 0.25 | 0.30 | 7 | 10 | 12 |
| D | 1.90 | 2.00 | 2.10 | 74 | 79 | 83 |
| D1 | | – | | | – | |
| D2 | 0.75 | 0.90 | 1.05 | 30 | 35 | 41 |
| E | 1.90 | 2.00 | 2.10 | 75 | 79 | 83 |
| E1 | | – | | | – | |
| E2 | 1.35 | 1.50 | 1.65 | 53 | 59 | 65 |
| e | 0.50 BSC | | | 20 BSC | | |
| L | 0.25 | 0.30 | 0.35 | 10 | 12 | 14 |

NOTE :

1. REFER TO JEDEC STD: MO–229.
2. DIMENSION "b" APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15MM AND 0.30MM FROM THE TERMINAL TIP. IF THE TERMINAL HAS OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION B SHOULD NOT BE MEASURED IN THAT RADIUS AREA.

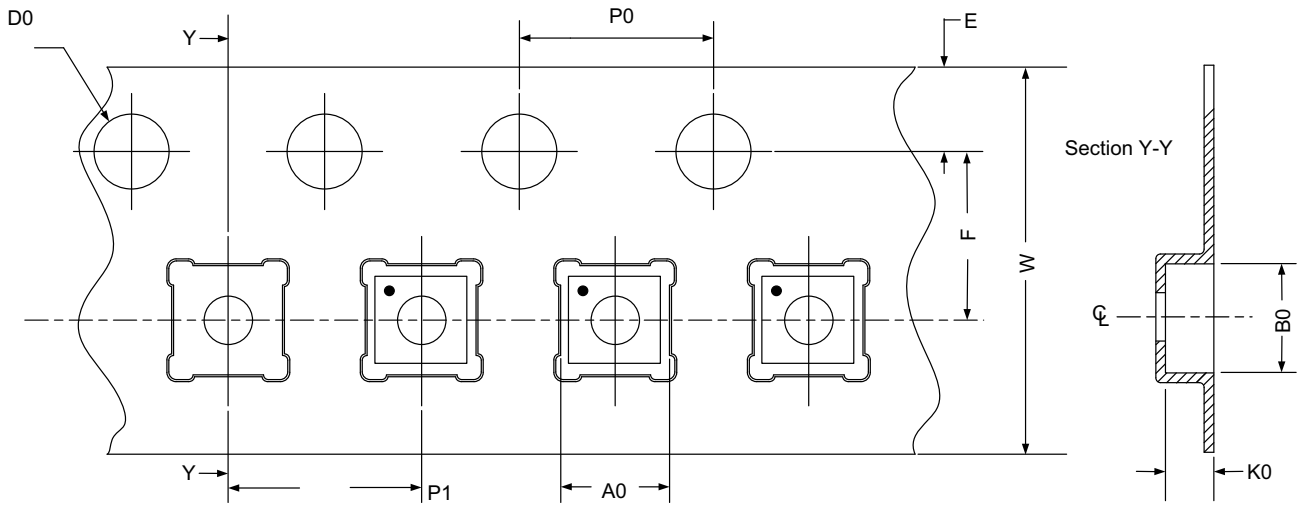
Note: Bottom side metal plate is at ground potential

## Tape and Reel Specifications

| Package Type | # of Pins | Nominal Package Size [mm] | Max Units | | Reel & Hub Size [mm] | Leader (min) | | Trailer (min) | | Tape Width [mm] | Part Pitch [mm] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | per Reel | per Box | | Pockets | Length [mm] | Pockets | Length [mm] | | |
| TDFN 8L Green | 8 | 2 x 2 x 0.75 | 3,000 | 3,000 | 178 / 60 | 100 | 400 | 100 | 400 | 8 | 4 |

## Carrier Tape Drawing and Dimensions

| Package Type | PocketBTM Length | PocketBTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|---|---|---|---|---|---|---|---|---|---|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | W |
| TDFN 8L Green | 2.3 | 2.3 | 1.05 | 4 | 4 | 1.55 | 1.75 | 3.5 | 8 |




## Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.00 $mm^3$ (nominal). More information can be found at www.jedec.org.

## Silego Website & Support

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For more information regarding Silego Green products, please visit:

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