# SLG8UM610

## Low Power Clock Synthesizer for Intel UMPC Systems

### Features

- CK610 compatible clock generator for Intel UMPC chipset
- Low Power differential CPU, SRC, LVDS_SSC and DOT_96 output buffers with integrated series terminations
- Three selectable CPU output frequencies - 100, 133, and 166MHz
- Up to 2.0% Spread Spectrum support for EMI reduction
- 100MHz LVDS_SSC clock support with additional spread spectrum options
- 1.5 Volt power supply
- 48 Pin QFN package (0.4mm pin pitch)

### Output Summary

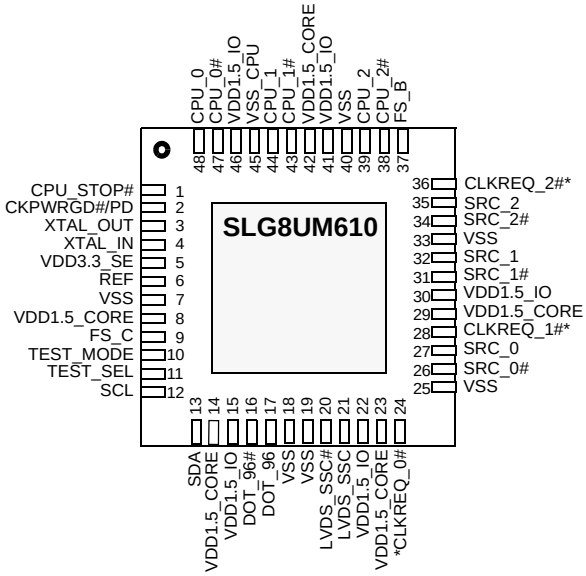
- 3 - LP differential CPU clock outputs @ 0.7V (with integrated termination)
- 1 - LP differential LVD_SSC clock output @ 0.7V (with integrated termination)
- 3 - LP differential Serial Reference Clock (SRC) clock outputs @ 0.7V (with integrated termination)
- 1 - LP differential 96MHz@ 0.7V (with integrated termination)
- 1 - single-ended 14.318MHz clock output @ 3.3V

**Table 1. CPU Frequency Select Table (FS_C, FS_B)**

| FS_C | FS_B | CPU (MHz) | SRC (MHz) | LVDS_SS (MHz) | REF (MHz) |
|---|---|---|---|---|---|
| 0 | 0 | 133.3 | 100.0 | 100.0 | 14.318 |
| 0 | 1 | 166.6 | 100.0 | 100.0 | 14.318 |
| 1 | 0 | 100.0 | 100.0 | 100.0 | 14.318 |
| 1 | 1 | 200.0 | 100.0 | 100.0 | 14.318 |

### Pin Configuration

(Top View)




* This pin has internal pull-up to VDD

48-Pin QFN
6.0x6.0mm body, 0.40mm pitch

Other brands and names may be claimed as the property of others

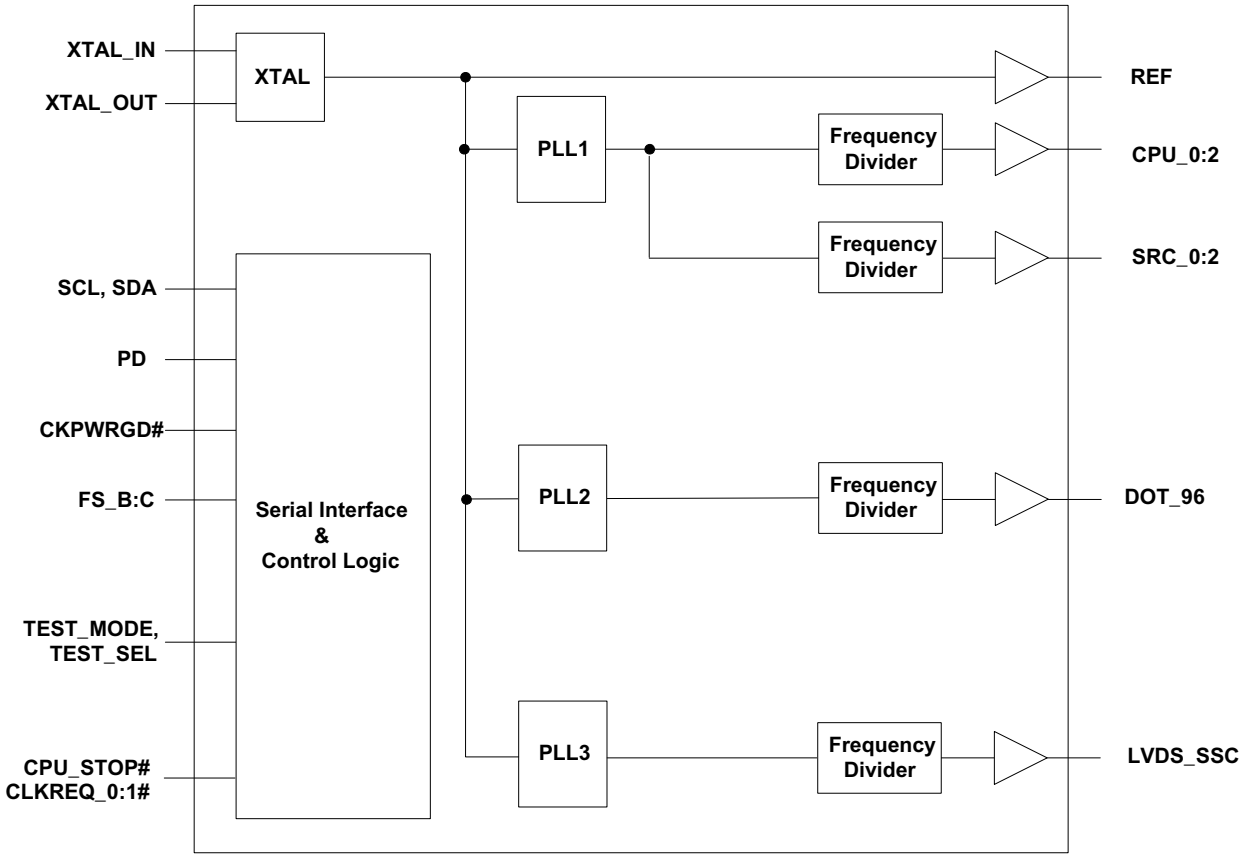
## Pin Description

| Pin # | Name | Type | Voltage (V) | Description |
|---|---|---|---|---|
| 1 | CPU_STOP# | I | 3.3V | 3.3V tolerant input to disable CPU clock outputs. |
| 2 | CKPWRGD#/PD | I | 3.3V | This level sensitive strobe determines when latch inputs are valid and are ready to be sampled. When high, this asynchronous input places the device into the power down state. |
| 3 | XTAL_OUT | O, SE | -- | 14.318MHz crystal output. |
| 4 | XTAL_IN | I | 1.5V | 14.318MHz crystal input. |
| 5 | VDD3.3_SE | PWR | 3.3V | 3.3V power supply for outputs. |
| 6 | REF | O, SE | -- | 14.318 reference clock output. |
| 7 | VSS | GND | -- | Ground for outputs. |
| 8 | VDD1.5_CORE | PWR | 1.5V | 1.5V power supply for PLL core. |
| 9 | FS_C | I | 1.5V | Frequency Select input to determine CPU output frequency. |
| 10 | TEST_MODE | I | 1.5V | 3.3V tolerant. When in test mode, TEST_MODE will configure outputs to run at Ref or Hi-Z. 0 = Hi-Z, 1 = Ref |
| 11 | TEST_SEL | I | 1.5V | 3.3V tolerant. When TEST_SEL input is pulled to 3.3V during VTT_PWRGD# assertion, the device will configure into TEST MODE. Refer to DC Parameters section for FS input voltage threshold. |
| 12 | SCL | I | 3.3V | Serial Interface bus clock input. |
| 13 | SDA | I/O, SE | 3.3V | Serial Interface bus data input and output. |
| 14 | VDD1.5_CORE | PWR | 1.5V | 1.5V power supply for PLL core. |
| 15 | VDD1.5_IO | PWR | 1.5V | 1.5V power supply for I/O. |
| 16 | DOT_96# | O, LP-DIF | 0.8V | Differential 96.000MHz Clock output. |
| 17 | DOT_96 | O, LP-DIF | 0.8V | Differential 96.000MHz Clock output. |
| 18 | VSS | GND | 0V | Ground for outputs. |
| 19 | VSS | GND | 0V | Ground for outputs. |
| 20 | LVDS_SSC# | O, LP-DIF | 0.8V | Differential 100.000MHz Clock Output with Spread Spectrum. |
| 21 | LVDS_SSC | O, LP-DIF | 0.8V | Differential 100.000MHz Clock Output with Spread Spectrum. |
| 22 | VDD1.5_IO | PWR | 1.5V | 1.5V power supply for I/O. |
| 23 | VDD1.5_CORE | PWR | 1.5V | 1.5V power supply for PLL core. |
| 24 | CLKREQ_0# | I | 1.5V | 1.5V tolerant input to control SRC_0 output. |
| 25 | VSS | GND | 0V | Ground for outputs. |
| 26 | SRC_0# | O, LP-DIF | 0.8V | Differential Serial Reference Clock output. |
| 27 | SRC_0 | O, LP-DIF | 0.8V | Differential Serial Reference Clock output. |
| 28 | CLKREQ_1# | I | 1.5V | 1.5V tolerant input to control SRC_1 output. |
| 29 | VDD1.5_CORE | PWR | 1.5V | 1.5V power supply for PLL core. |
| 30 | VDD1.5_IO | PWR | 1.5V | 1.5V power supply for I/O. |
| 31 | SRC_1# | O, LP-DIF | 0.8V | Differential Serial Reference Clock output. |
| 32 | SRC_1 | O, LP-DIF | 0.8V | Differential Serial Reference Clock output. |

## Pin Description (continued)

| Pin # | Name | Type | Voltage (V) | Description |
|---|---|---|---|---|
| 33 | VSS | GND | 0V | Ground for outputs. |
| 34 | SRC_2# | O, LP-DIF | 0.8V | Differential Serial Reference Clock output. |
| 35 | SRC_2 | O, LP-DIF | 0.8V | Differential Serial Reference Clock output. |
| 36 | CLKREQ_2# | I | 1.5V | 1.5V tolerant input to control SRC_2 output. |
| 37 | FS_B | I | 1.5V | Frequency Select input to determine CPU output frequency. |
| 38 | CPU_2# | O, LP-DIF | 0.8V | Differential CPU Clock output. |
| 39 | CPU_2 | O, LP-DIF | 0.8V | Differential CPU Clock output. |
| 40 | VSS | GND | 0V | Ground for outputs. |
| 41 | VDD1.5_IO | PWR | 1.5V | 1.5V power supply for I/O. |
| 42 | VDD1.5_CORE | PWR | 1.5V | 1.5V power supply for PLL core. |
| 43 | CPU_1# | O, LP-DIF | 0.8V | Differential CPU Clock output. |
| 44 | CPU_1 | O, LP-DIF | 0.8V | Differential CPU Clock output. |
| 45 | VSS_CPU | GND | 0V | Ground for outputs. |
| 46 | VDD1.5_IO | PWR | 1.5V | 1.5V power supply for I/O. |
| 47 | CPU_0# | O, LP-DIF | 0.8V | Differential CPU Clock output. |
| 48 | CPU_0 | O, LP-DIF | 0.8V | Differential CPU Clock output. |

## Block Diagram



## Type “SR” differential output buffer with integrated series termination

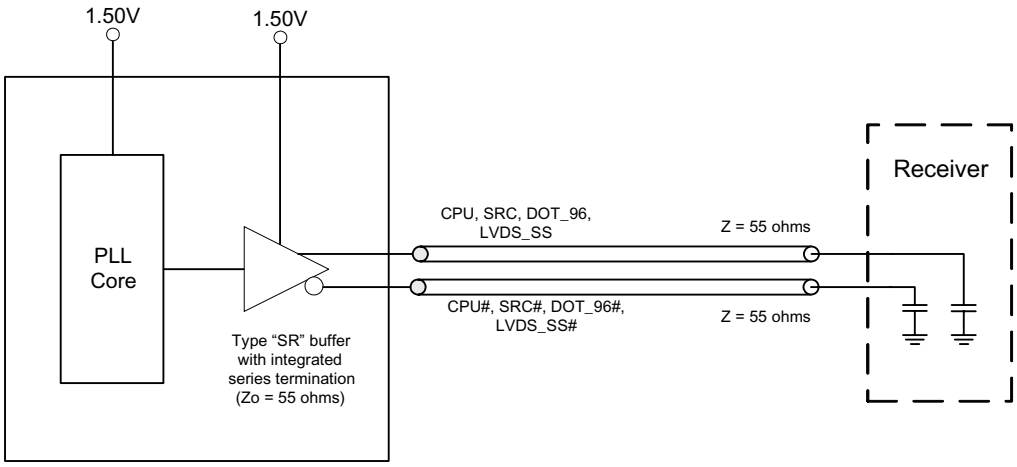



**Figure 1. Type “SR” differential output buffer with integrated series termination.**

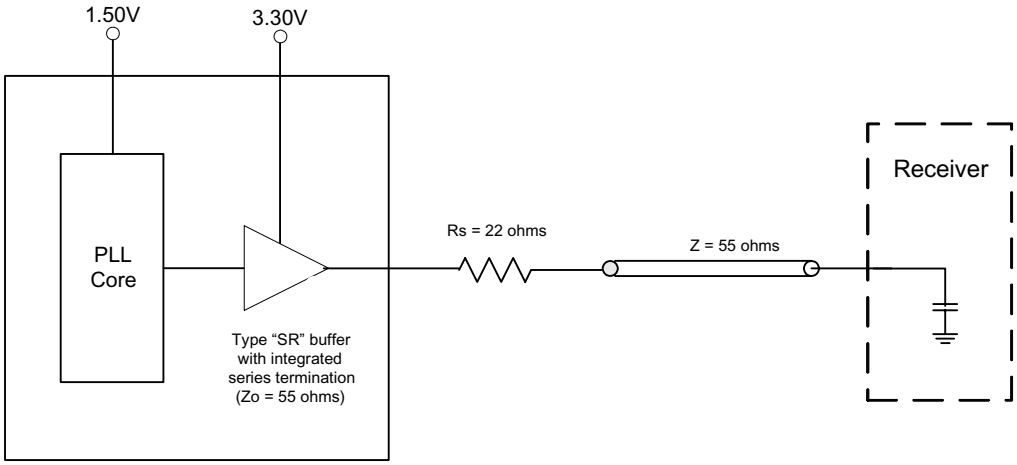



**Figure 2. Single-ended Clock Layout Topology.**

## Frequency Select Pins (FS_B, FS_C)

Host clock frequency selection is achieved by applying the appropriate logic levels to Frequency Select (FS) inputs prior to CKPWRGD# assertion (as seen by the clock synthesizer). Upon CKPWRGD# being sampled low by the clock chip (indicating processor VTT voltage is stable), the clock chip samples the FS input values. CKPWRGD# employs a one-shot functionality in that once a valid low on CKPWRGD# has been sampled, all further CKPWRGD#, FS input transitions will be ignored. Please refer to Frequency Select Table for different CPU frequency configurations.

## TEST_SEL Hardware Control Via TEST_MODE pin

Once test clock operation has been invoked, the TEST_MODE pin will select between the Hi-Z and REF mode as shown in the table below.

**Table 2. Test Mode Selection Table**

| TEST_MODE | CPU | SRC | LVDS_SSC | REF | DOT_96 |
|---|---|---|---|---|---|
| 1 | REF | REF | REF | REF | REF |
| 0 | Hi-Z | Hi-Z | Hi-Z | Hi-Z | Hi-Z |

## PD (Power Down) Clarification

The CKPWRGD#/PD pin is a dual function pin. During initial power-up, the pin functions as CKPWRGD#. Once CKPWRGD# has been sampled low by the device, the pin assumes PD functionality. The PD pin is an asynchronous active high input. When PD is asserted high, all single ended clock outputs are disabled. The VCOs and the crystal oscillator are then turned off.

**Table 3. PD Functionality**

| PD | CPU | CPU# | LVDS_SSC | LVDS_SSC# | DOT_96 | DOT_96# | REF |
|---|---|---|---|---|---|---|---|
| 0 | Normal | Normal | Normal | Normal | Normal | Normal | Normal |
| 1 | Low | Low | Low | Low | Low | Low | Low |

### PD Assertion

When PD is sampled high by two consecutive rising edges of CPU#, all single-ended outputs will be driven low on their next high to low transition and differential clocks will be disabled.

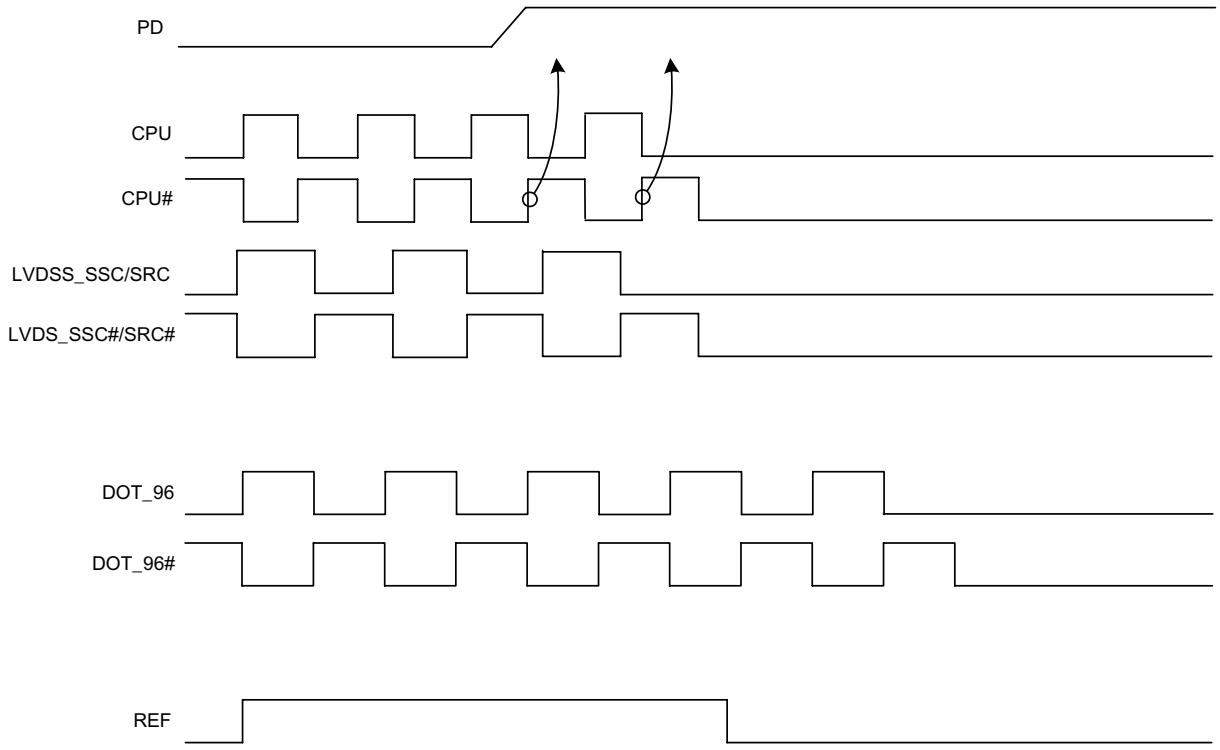



**Figure 3. PD Assertion**

**PD De-assertion**

The power-up latency is less than 1.8ms. This is the time from the de-assertion of the PD pin or the ramping of the power supply until the time that stable clocks are output from the clock device.

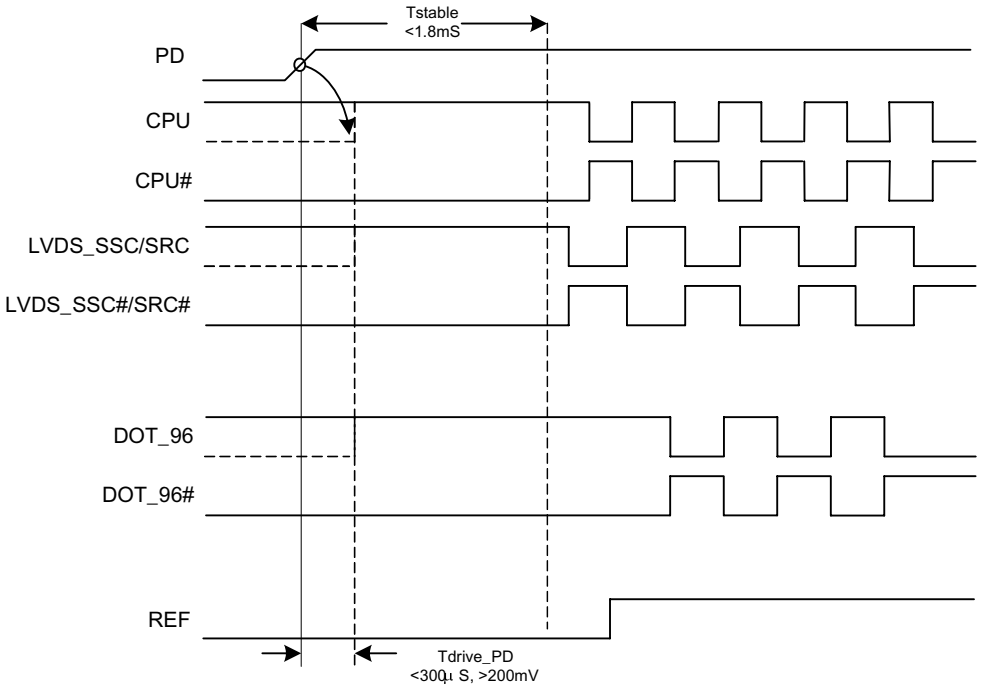



**Figure 4. PD De-assertion**

## CKPWRGD# Operation

CKPWRGD# is an active low signal to indicate when the processor VTT voltage has stabilized. The significance of the VTT supply being stable is that only after VTT is stable are the processor frequency select (FS) and VID bits become valid.

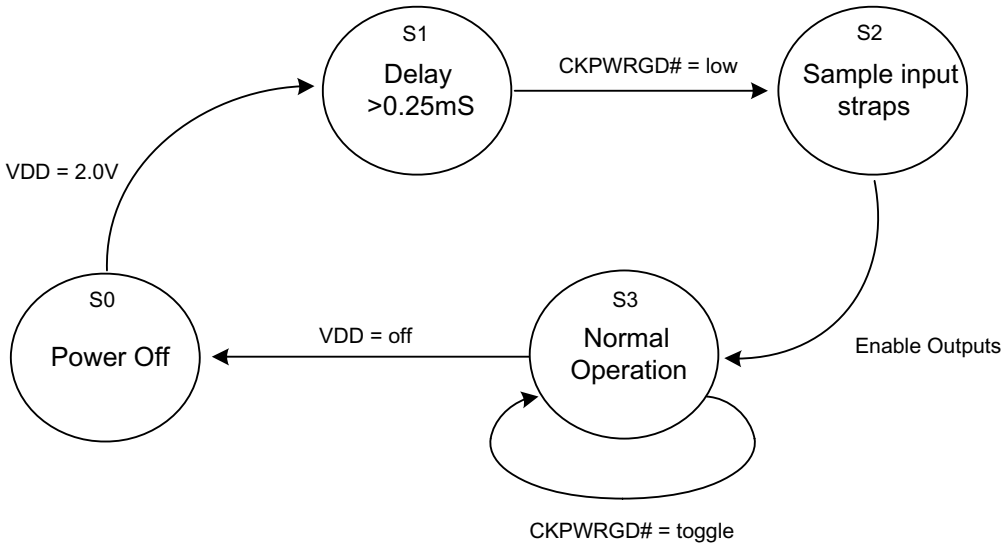



**Figure 5. Clock Generator Power Up/Run State Diagram**

## CPU_STOP# Clarification

The CPU_STOP# signal is an active low asynchronous input used for cleanly stopping and starting the CPU outputs while the rest of the clock generator continues to function.

**Table 4. CPU_STOP# Functionality**

| CPU_STOP# | CPU | CPU# | SRC/ LVDS_SSC | SRC#/ LVDS_SSC# | DOT_96 | DOT_96# | REF |
|---|---|---|---|---|---|---|---|
| 1 | Normal | Normal | Normal | Normal | Normal | Normal | Normal |
| 0 | High | Low | Normal | Normal | Normal | Normal | Normal |

## CPU_STOP# Assertion (Transition from '1' to '0')

When CPU_STOP# is asserted, all CPU outputs that are set in the control registers to be stoppable are to be stopped between 2~6 CPU clock periods.

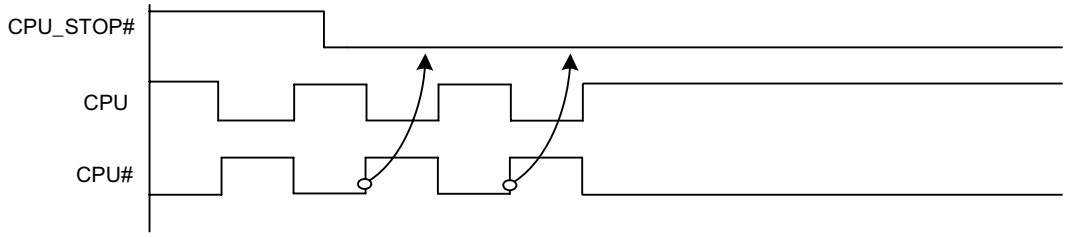



**Figure 6. Assertion of CPU_STOP#**

## CPU_STOP# De-Assertion (Transition from '0' to '1')

All differential outputs that were stopped are to resume normal operation in a glitch free manner. The maximum latency from the de-assertion to active outputs is between 2-6 CPU clock periods.

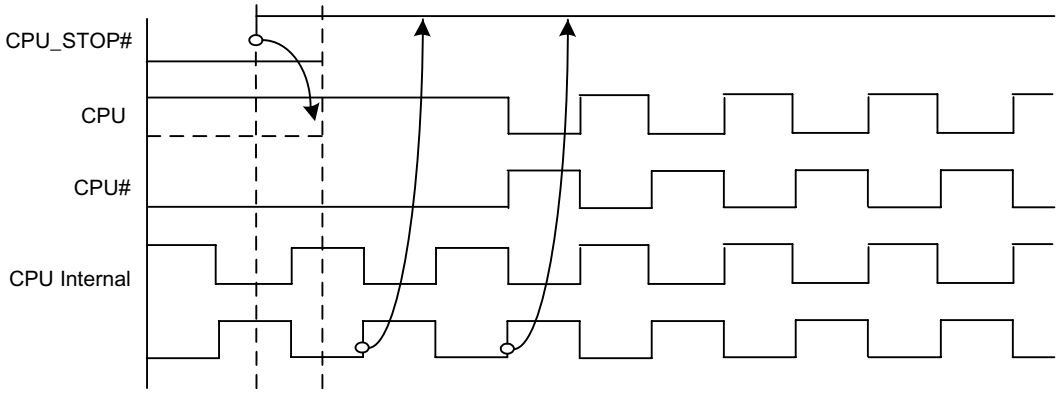



**Figure 6. CPU_STOP# De-Assertion**

## Serial Bus Interface

A two-wire serial interface is provided as the programming interface for the clock synthesizer. The serial interface is fully compliance to the SMBus 2.0 specification. The registers associated with the two-wire interface initializes to their default setting upon power-up, and therefore use of this interface is optional.
The serial interface supports block write and block read operation from any SMBus master devices. For block write and block read operations, the bytes must be accessed in sequential order from lowest to highest byte (most significant bit first) with the ability to stop after any complete byte has been transferred. The block write and block read protocol is outlined in *Table 5*. The slave receiver address is 11010010 (D2h).

**Table 5. Block Read and Block Write protocol**

| Block Write Protocol | | Block Read Protocol | |
|---|---|---|---|
| **Bit** | **Description** | **Bit** | **Description** |
| 1 | Start | 1 | Start |
| 2:8 | Slave address - 7 bits | 2:8 | Slave address - 7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 11:18 | Command Code - 8 Bit<br>'00000000' stands for block operation | 11:18 | Command Code - 8 Bit<br>'00000000' stands for block operation |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 20:27 | Byte Count - 8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 21:27 | Slave address - 7 bits |
| 29:36 | Data byte 0 - 8 bits | 28 | Read |
| 37 | Acknowledge from slave | 29 | Acknowledge from slave |
| 38:45 | Data byte 1 - 8 bits | 30:37 | Byte count from slave - 8 bits<br>(Byte count = 21) |
| 46 | Acknowledge from slave | 38 | Acknowledge |
| .... | Data Byte N/Slave Acknowledge... | 39:46 | Data byte from slave - 8 bits |
| .... | Data Byte N - 8 bits | 47 | Acknowledge |
| .... | Acknowledge from slave | 48:55 | Data byte from slave - 8 bits |
| .... | Stop | 56 | Acknowledge |
| | | .... | Data bytes from slave/Acknowledge |
| | | .... | Data byte N from slave - 8 bits |
| | | .... | Not Acknowledge |
| | | .... | Stop |

**Table 6. Byte Read and Byte Write protocol**

| Byte Write Protocol | | Byte Read Protocol | |
|---|---|---|---|
| **Bit** | **Description** | **Bit** | **Description** |
| 1 | Start | 1 | Start |
| 2:8 | Slave address - 7 bits | 2:8 | Slave address - 7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 11:18 | Command Code - 8 bits<br>'1xxxxxxx' stands for byte operation<br>bit[6:0] of the command code represents the offset of the byte to be accessed | 11:18 | Command Code - 8 bits<br>'1xxxxxxx' stands for byte operation<br>bit[6:0] of the command code represents the offset of the byte to be accessed |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 20:27 | Data byte 0 - 8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 21:27 | Slave address - 7 bits |
| 29 | Stop | 28 | Read |
| | | 29 | Acknowledge from slave |
| | | 30:37 | Data byte from slave - 8 bits |
| | | 38 | Not Acknowledge |
| | | 39 | Stop |

## Control Register Summary

### Control Register 0

| Bit | Type | Description/Function | Power up condition |
|---|---|---|---|
| 7 | RW | PLL1 Enable<br>0 = Disabled<br>1 = Enabled | 1 |
| 6 | RW | PLL2 Enable<br>0 = Disabled<br>1 = Enabled | 1 |
| 5 | RW | PLL3 Enable<br>0 = Disabled<br>1 = Enabled | 1 |
| 4 | R | Reserved | 0 |
| 3 | RW | CPU Output Divider Enable<br>0 = Disabled<br>1 = Enabled<br>*Note: This bit should be automatically set to '0' if bit 7 is set to '0'* | 1 |
| 2 | RW | SRC Output Divider Enable<br>0 = Disabled<br>1 = Enabled<br>*Note: This bit should be automatically set to '0' if bit 7 is set to '0'* | 1 |
| 1 | RW | SSC(LVDS) Output Divider Enable<br>0 = Disabled<br>1 = Enabled<br>*Note: This bit should be automatically set to '0' if bit 5 is set to '0'* | 1 |
| 0 | RW | DOT Output Divider Enable<br>0 = Disabled<br>1 = Enabled<br>*Note: This bit should be automatically set to '0' if bit 6 is set to '0'* | 1 |

### Control Register 1

| Bit | Type | Description/Function | Power up condition |
|---|---|---|---|
| 7 | RW | PLL1 Spread Spectrum Enable<br>0 = Disabled<br>1 = Enabled | 1 |
| 6 | RW | PLL3 Spread Spectrum Enable<br>0 = Disabled<br>1 = Enabled | 1 |
| 5:3 | RW | PLL3 Spread Spectrum Frequency Select<br>000 = 0.50% (Down-Spread)<br>001 = 1.00% (Down-Spread)<br>010 = 1.50% (Down-Spread)<br>011 = 2.00% (Down-Spread)<br>100 = ±0.30% (Center-Spread)<br>101 = ±0.50% (Center-Spread)<br>110 = ±0.75% (Center-Spread)<br>111 = ±1.00% (Center-Spread) | 000 |
| 2:0 | R | Reserved | 000 |

**Control Register 2**

| Bit | Type | Description/Function | Power up condition |
|---|---|---|---|
| 7 | RW | CPU_0 Output Buffer Enable<br>0 = Disabled<br>1 = Enabled | 1 |
| 6 | RW | CPU_1 Output Buffer Enable<br>0 = Disabled<br>1 = Enabled | 1 |
| 5 | RW | CPU_2 Output Buffer Enable<br>0 = Disabled<br>1 = Enabled | 1 |
| 4 | RW | SRC_0 Output Buffer Enable<br>0 = Disabled<br>1 = Enabled | 1 |
| 3 | RW | SRC_1 Output Buffer Enable<br>0 = Disabled<br>1 = Enabled | 1 |
| 2 | RW | SRC_2 Output Buffer Enable<br>0 = Disabled<br>1 = Enabled | 1 |
| 1 | RW | DOT_0 Output Buffer Enable<br>0 = Disabled<br>1 = Enabled | 1 |
| 0 | RW | LVDS Output Buffer Enable<br>0 = Disabled<br>1 = Enabled | 1 |

**Control Register 3**

| Bit | Type | Description/Function | Power up condition |
|---|---|---|---|
| 7 | RW | Reserved | 0 |
| 6 | RW | Reserved | 0 |
| 5 | RW | REF Output Buffer Enable<br>0 = Disabled<br>1 = Enabled | 1 |
| 4 | RW | REF Drive Strength<br>0 = 1 Load<br>1 = 2 Loads | 1 |
| 3 | R | Reserved | 0 |
| 2 | RW | CPU_0 Control from CPU_STOP#<br>0 = Free Running<br>1 = Stopped | 0 |
| 1 | RW | CPU_1 Control from CPU_STOP#<br>0 = Free Running<br>1 = Stopped | 0 |
| 0 | RW | CPU_2 Control from CPU_STOP#<br>0 = Free Running<br>1 = Stopped | 0 |

**Control Register 4**

| Bit | Type | Description/Function | Power up condition |
|---|---|---|---|
| 7:0 | R | Reserved | 00000000 |

**Control Register 5**

| Bit | Type | Description/Function | Power up condition |
|---|---|---|---|
| 7:0 | R | Reserved | 00000000 |

**Control Register 6**

| Bit | Type | Description/Function | Power up condition |
|---|---|---|---|
| 7:0 | R | Reserved | 00000000 |

**Control Register 7**

| Bit | Type | Description/Function | Power up condition |
|---|---|---|---|
| 7:0 | R | Reserved | 00000000 |

**Control Register 8**

| Bit | Type | Description/Function | Power up condition |
|---|---|---|---|
| 7:0 | R | Reserved | 00000000 |

**Control Register 9**

| Bit | Type | Description/Function | Power up condition |
|---|---|---|---|
| 7:0 | R | Reserved | 00000000 |

**Control Register 10**

| Bit | Type | Description/Function | Power up condition |
|---|---|---|---|
| 7 | R | FS_B Status | X |
| 6 | R | FS_C Status | X |
| 5:3 | R | CLKREQ_0:2# Status | XXX |
| 2:0 | R | Reserved | 000 |

**Control Register 11**

| Bit | Type | Description/Function | Power up condition |
|---|---|---|---|
| 7 | R | Revision ID bit 3 | 0 |
| 6 | R | Revision ID bit 2 | 0 |
| 5 | R | Revision ID bit 1 | 0 |
| 4 | R | Revision ID bit 0 | 0 |

**Control Register 11**

| Bit | Type | Description/Function | Power up condition |
|---|---|---|---|
| 3 | R | Vendor ID bit 3 | 0 |
| 2 | R | Vendor ID bit 2 | 1 |
| 1 | R | Vendor ID bit 1 | 1 |
| 0 | R | Vendor ID bit 0 | 0 |

**Control Register 12**

| Bit | Type | Description/Function | Power up condition |
|---|---|---|---|
| 7 | R | Device ID bit 3 | 0 |
| 6 | R | Device ID bit 2 | 0 |
| 5 | R | Device ID bit 1 | 0 |
| 4 | R | Device ID bit 0 | 0 |
| 3 | R | Reserved | 0 |
| 2 | R | Reserved | 0 |
| 1 | R | Reserved | 0 |
| 0 | R | Reserved | 0 |

**Control Register 13**

| Bit | Type | Description/Function | Power up condition |
|---|---|---|---|
| 7:0 | R | Reserved | 00000000 |

**Control Register 14**

| Bit | Type | Description/Function | Power up condition |
|---|---|---|---|
| 7:0 | R | Reserved | 00000000 |

**Control Register 15**

| Bit | Type | Description/Function | Power up condition |
|---|---|---|---|
| 7:0 | RW | Byte Count register for block read operation<br>Note: The default value is 16. To read more than 16 bytes, system BIOS needs to change this register to the number of bytes it intends to read. | 00010000 |

**Control Register 16 to 21 (Reserved)**

| Bit | Type | Description/Function | Power up condition |
|---|---|---|---|
| 7:0 | R | Reserved | 00000000 |

## Crystal Recommendations

The SLG8UM610 requires a **Parallel Resonance Crystal.** Substituting a series resonance crystal will cause the SLG8UM610 to operate at the wrong frequency and violate the ppm specification. For most applications there is a 300ppm frequency shift between series and parallel crystals due to incorrect loading.

**Table 7. Crystal Recommendations.**

| Frequency (Fund) | Cut | Loading | Load Cap | Drive (max.) | Shunt Cap (max.) | Motional (max.) | Cut Accuracy (max.) | Temp Stability (max.) | Aging (max.) |
|---|---|---|---|---|---|---|---|---|---|
| 14.31818MHz | AT | Parallel | 20pF | 0.1mW | 5pF | 0.016pF | 35ppm | 30ppm | 5ppm |

## Absolute Maximum Ratings

Storage Temperature:–65°C to + 150°C

Supply Voltage (VDDA):TBD

Supply Voltage (VDD):TBD

3.3V Input Voltage:-0.5 to 4.6V

Operating Temperature (Ambient):0°C to +70°C

ESD Protection (Min):2000V

Lead Frame Material (for Green package): Sn/Bi

Reflow Temperature (for Green package): 260°C (10sec)

## DC Electrical Characteristics

### Operating Conditions

| Symbol | Description | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VDD_CORE | 1.5V Core Supply Voltage | 1.5V±5% | 1.425 | | 1.575 | V |
| VDD | 3.3V I/O Supply Voltage | 3.3V±5% | 3.135 | | 3.465 | V |
| Vih | 3.3V Input High Voltage | VDD | 2.0 | | VDD+0.3 | V |
| Vil | 3.3V Input Low Voltage | | VSS-0.3 | | 0.8 | V |
| Vih_FS | 3.3V Input High Voltage | VDD | 0.7 | | VDD+0.3 | V |
| Vil_FS | 3.3V Input Low Voltage | | VSS-0.3 | | 0.35 | V |
| Voh | 3.3V Output High Voltage | Ioh = -1mA | 2.4 | | | V |
| Vol | 3.3V Output Low Voltage | Iol = 1mA | | | 0.4 | V |
| Iil | Input Leakage Current | 0 < Vin < VDD | -5 | | +5 | uA |
| Cin | Input Pin Capacitance | | 1.5 | | 5 | pF |
| Cxtal | Xtal Pin Capacitance | | 3 | | 5 | pF |
| Cout | Output Pin Capacitance | | | | 6 | pF |
| Lpin | Pin Inductance | | | | 7 | nH |
| P_ON | Power Consumption | All 3 PLLs locked and running with spread spectrum disabled.<br>+V1.5_CORE = 1.5V<br>+V_DIFF_IO = 1.5V<br>+V3.3_IO = 3.3V<br>CPU = 133 MHz<br>SRC = 100MHz<br>DOT = 96 MHz<br>LVDS = 100 MHz<br>REF = 14.318 MHz<br>All clock outputs are driving test case lump loads. | | | 100 | mW |

## AC Electrical Characteristics

### Differential Outputs (CPU, SRC, LVDS_SSC, DOT_96) Timing Characteristics

| Symbol | Description | Min. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| Laccurracy | Long term accuracy (CPU, SRC) | | 300 | ppm | Using frequency counter with the measurement interval equal or greater than 0.15 second |
| Laccurracy | Long term accuracy (LVDS_SS, DOT_96) | | 100 | ppm | Using frequency counter with the measurement interval equal or greater than 0.15 second |
| Tperiod | Average CPU Period (100MHz, SSC disabled) | 9.997001 | 10.003000 | ns | Average period over 1 us |
| Tperiod | Average CPU Period (133MHz, SSC disabled) | 7.497751 | 7.502251 | ns | Average period over 1 us |
| Tperiod | Average CPU Period (166MHz, SSC disabled) | 5.998201 | 6.001801 | ns | Average period over 1 us |
| Tperiod | Average CPU Period (100MHz, SSC enabled) | 9.997001 | 10.05327 | ns | Average period over 1 us |
| Tperiod | Average CPU Period (133MHz, SSC enabled) | 7.497751 | 7.539950 | ns | Average period over 1 us |
| Tperiod | Average CPU Period (166MHz, SSC enabled) | 5.998201 | 6.031960 | ns | Average period over 1 us |
| Tperiod | Average SRC/LVDS_SSC Period (100MHz, SSC disabled) | 9.997001 | 10.003000 | ns | Average period over 1 us |
| Tperiod | Average SRC/LVDS_SSC Period (100MHz, SSC enabled) | 9.997001 | 10.05327 | ns | Average period over 1 us |
| Tperiod | Average DOT_96 Period (96MHz) | 10.41354 | 10.41979 | ns | Average period over 1 us |
| Tabs | Absolute Min/Max CPU Period (100, SSC disabled) | 9.912001 | 10.08800 | ns | |
| Tabs | Absolute Min/Max CPU Period (133, SSC disabled) | 7.412751 | 7.587251 | ns | |
| Tabs | Absolute Min/Max CPU Period (166, SSC disabled) | 5.913201 | 6.086801 | ns | |
| Tabs | Absolute Min/Max CPU Period (100, SSC enabled) | 9.912001 | 10.13827 | ns | |
| Tabs | Absolute Min/Max CPU Period (133, SSC enabled) | 7.412751 | 7.624950 | ns | |
| Tabs | Absolute Min/Max CPU Period (166, SSC enabled) | 5.913201 | 6.116960 | ns | |
| Tabs | Absolute Min/Max SRC/LVDS_SSC Period (100, SSC disabled) | 9.872001 | 10.12800 | ns | |
| Tabs | Absolute Min/Max SRC/LVDS_SSC Period (100, SSC enabled) | 9.872001 | 10.17827 | ns | |
| Tabs | Absolute Min/Max DOT_96 Period (96MHz) | 10.16354 | 10.66979 | ns | |
| Slew_rise | Rising slew rate | 0.6 | 4.0 | V/ns | Measured through V_swing voltgae centered about differential zero.<br>Measured on a component test board. |
| Slew_fall | Falling slew rate | 0.6 | 4.0 | V/ns | Measured through V_swing voltgae centered about differential zero.<br>Measured on a component test board. |
| V_swing | Differential output swing | 300 | | mV | Measurement taken from differential waveform on a component test board |
| V_cr | Crossing point voltage | 300 | 550 | mV | The voltage where Clock=Clock#, measured on a component test board. Measurement taken from single ended waveform. |
| V_cr_dlt | Variation of V_cr | | 140 | mV | It is defined as the total variation of all crossing voltages of Rising Clock and Falling Clock#.Measured on a component test board. Measurement taken from single ended waveform. |
| Tccjitter | Cycle to Cycle Jitter (CPU) | | 85 | ps | |
| Tccjitter | Cycle to Cycle Jitter (SRC) | | 85 | ps | |
| Tccjitter | Cycle to Cycle Jitter (DOT_96, LVDS_SS) | | 250 | ps | |
| Duty Cycle | Duty Cycle | 45 | 55 | % | |

### Differential Outputs (CPU, SRC, LVDS_SSC, DOT_96) Timing Characteristics

| Symbol | Description | Min. | Max. | Unit | Conditions |
|---|---|---|---|---|---|
| V_max | Maximum output voltage | | 1.15 | V | Measurement taken from single ended waveform on a component test board. The max voltage including overshoot. |
| V_min | Minimum output voltage | -0.3 | | V | Measurement taken from single ended waveform on a component test board.The minimum voltage including undershoot |
| Vrb | Ringback Voltage | | 0.2 | V | |
| Tskew | Pin-to-Pin Skew (CPU_0:2) | | 100 | ps | |
| Tskew | Pin-to-Pin Skew (all SRC outputs) | | 250 | ps | |

### REF Timing Characteristics

| Symbol | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| Laccurracy | Long term accuracy | | 95 | ppm | Using frequency counter with the measurement interval equal or greater than 0.15 second |
| Tperiod | Average Period | 69.82033 | 69.86224 | ns | Average period over 1 us |
| Tabs | Absolute Min/Max Period | 68.82033 | 70.86224 | ns | |
| Thigh | CLK high time | 20 | 50 | ns | |
| Tlow | CLK low time | 20 | 50 | ns | |
| Edge Rate | Rising edge rate | 1.0 | 4.0 | V/ns | Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system |
| Edge Rate | Falling edge rate | 1.0 | 4.0 | V/ns | Measured from 0.4V to 2.4V in test board, measured from 0.8V to 2.0V in system |
| Tccjitter | Cycle to cycle jitter | | 1000 | ps | |
| Duty Cycle | Duty Cycle | 45 | 55 | % | |

## Ordering Information

| Part Number | Package Type | Temperature Range |
|---|---|---|
| SLG8UM610V | 48-pin QFN | Commercial, 0° to 70°C |
| SLG8UM610VTR | 48-pin QFN - Tape and Reel | Commercial, 0° to 70°C |

## Package Drawing and Dimensions

### 48 Pin QFN Package

**Package Type: TQFN 6x6 48L**

| Unit: mm | Silego Spec (Comply to JEDEC MO-220) Dimension in MM | | |
|---|---|---|---|
| Symbol | Min | NOM | Max |
| A | 0.80 | 0.85 | 1.00 |
| A1 | 0.00 | - | 0.05 |
| A2 | - | 0.65 | 1.00 |
| A3 | | 0.20 REF | |
| b | 0.15 | 0.20 | 0.25 |
| D | | 6.00 BSC | |
| E | | 6.00 BSC | |
| D1 | | 5.75 BSC | |
| E1 | | 5.75 BSC | |
| D2 | 2.85 | - | 3.15 |
| E2 | 2.85 | - | 3.15 |
| e | | 0.40 BSC | |
| L | 0.30 | 0.40 | 0.50 |
| θ (Degree) | 0 | - | 14 |